NAT'L INST. OF STAND & TECH R.I.C.
A11105 355573

NIST
PUBLICATIONS

NISTIR 5851

Project Portfolio FY 1998

The National Semiconductor Metrology Program

QC
100
.U56
NO.5851
1998

Edited by

Stephen Knight
and Alice Settle-Raskin
Office of Microelectronics Programs

U.S. DEPARTMENT OF COMMERCE

Technology Administration

National Institute of Standards and Technology

Revised March 1998

NIST

NISTIR 5851

Project Portfolio FY 1998

The National Semiconductor Metrology Program

Edited by

Stephen Knight
and Alice Settle-Raskin
Office of Microelectronics Programs

U.S. DEPARTMENT OF COMMERCE
William M. Daley, Secretary

Technology Administration
Gary R. Bachula, Acting Under Secretary for Technology

National Institute of Standards and Technology
Raymond G. Kammer, Director

Revised March 1998

Foreword

The National Semiconductor Metrology Program (NSMP) is a NIST-wide effort designed to meet the highest priority measurement needs of the semiconductor industry as expressed by the *National Technology Roadmap for Semiconductors* and other authoritative industry sources. The NSMP was established in 1994 with a strong focus on mainstream silicon CMOS technology and an ultimate funding goal of $25 million annually. Current annual funding of approximately $11 million supports the 29 internal projects which are summarized in this Project Portfolio booklet.

The NSMP is operated by NIST's Office of Microelectronics Programs, which also manages NIST's relationships with the Semiconductor Industry Association (SIA), SEMATECH, and the Semiconductor Research Corporation (SRC). These include NIST's memberships on the SIA committees that develop the *National TechnologyRoadmap for Semiconductors* and numerous SRC technical management committees. In addition, NIST is active in the semiconductor standards development activities of American Society for Testing and Materials (ASTM), Deutsches Institut für Normung (DIN), Electronic Industries Association (EIA), International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI).

For further information about our program or how we can serve you, please contact us as follows:

Office of Microelectronics Programs
National Institute of Standards and Technology
Building 225, Room A323
Gaithersburg, MD 20899-0001
phone: (301) 975-4400
fax: (301) 948-0978
e-mail: nsmp@nist.gov
http://www.eeel.nist.gov/omp

Please note:

Disclaimer: Certain commercial equipment and/or software is identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the *National Technology Roadmap for Semiconductors* (NTRS) apply to the most recent edition, dated 1997. This document is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600, fax: (408) 436-6646.

Table of Contents

Foreword iii

Disclaimer and References Note iv

Table of Contents v

Lithography

1. Dimensional Metrology at the Nanometer Level: Combined SEM/PPM 1
2. Nanometer Scale Metrology With Atomic Force Microscopy 2
3. Linewidth Correlation 3
4 Electrical Linewidth and Overlay Metrology 4
5. Optical CD and Overlay Metrology 5
6. High-Accuracy Two-Dimensional Measurements 6
7. Radiometric Metrology for Deep Ultraviolet Lithography 7
8. Deep Ultraviolet Laser Metrology for Semiconductor Photolithography 8

Processing

9. Fundamental Process Control Metrology for Gases 9
10. Low Concentration Humidity Standards 10
11. Plasma and CVD Process Measurements 11
12. Metrology for Contamination-Free Manufacturing 12
13. Highly Accurate Thermometry for Semiconductor Processing Using Pure Element Thermocouples .. 13
14. Temperature Measurement for Rapid Thermal Processing 14
15. Particle Measurements in Support of the Semiconductor Industry 15
16. Optical Scattering for Wafer Surface Metrology 16
17. High-Resolution X-Ray Spectrometer for Chemical Analysis 17
18. Chemical Characterization of Thin Films and Particle Contaminants 18

Front-End Processes

19. Wafer and Chuck Flatness/Thickness 19
20. Measurements and Standards for Thin Dielectric Films 20
21. Scanning Probe Microscopy for Dopant Profiling 21
22. Thin-Film Profile Measurement Methods and Reference Materials 22
23. Ultra-Thin Dielectric Reliability Metrology 23

Interconnect

24. Interconnect Materials and Reliability Metrology 25
25. Thin-Film Characterization from Transmission-Line Measurement 26

Packaging

26. Experimental Micromechanics by e-Beam Moiré 27
27. Hygrothermal Expansion of Polymer Thin Films 28
28. Solderability Measurements for Microelectronics 29

Design

29. Metrology for Simulation and Computer Aided Design 31

Appendix A: Abbreviations and Acronyms 33

Appendix B: Key Words Index 35

Appendix C: Recent Publications 39

LITHOGRAPHY

Dimensional Metrology at the Nanometer Level: Combined SEM/PPM

The scanning electron microscope (SEM) has become the familiar instrument of choice for in-line process inspection and metrology. Scanning proximal probe (PPM) instruments such as the atomic force and scanning tunneling microscopes have recently emerged to both complement and extend the capabilities of the SEM. NIST is exploring the potentials provided by a tool which is unique through the marriage of a compact scanned probe instrument with a high-resolution field emission SEM. The proof-of-concept work is being facilitated through a CRADA with a commercial scanned probe instrument company. The combination of these two techniques is expected to yield an instrument with superior qualitative and quantitative capabilities which will be a great aid in the development of standards for semiconductor manufacturing. This is the first step in the development of a NIST "measurement engine" for advanced microelectronics. The two commercial instruments have been combined and tested. Improvements to the instruments for this unique application have been recommended to the manufacturer, and the findings were reported in recent publications.[1, 2]

This project consists of five elements: (1) Acquisition, delivery, and installation of the high resolution field emission SEM and the PPM systems; (2) use and data acquisition; (3) optimization of the systems and incorporation of improvements; (4) use of the improved system in the development of standards; and (5) construction of a combined NIST instrument.

The SEM and the PPM were installed and were functional during FY 1997. Improvements were recommended to the PPM manufacturer in order to enhance functionality in the high resolution SEM environment. Data using RM 8090 (the prototype SEM magnification calibration standard) and SRM 2091 (the prototype SEM sharpness standard) were taken, and the results presented at three technical meetings.

The PPM will be returned to the manufacturer during FY 1998 for extensive modifications and then will be re-installed in the SEM.

Metrology is mentioned throughout the Lithography chapter of the 1997 National Technology Roadmap for Semiconductors (NTRS). Requirements are defined on page 94, Table 28. Potential solutions are on page 95, Figure 22. Metrology is cited as one of the grand challenges on pages 11 and 12.

Contact: Dr. Michael T. Postek, phone: (301) 975-2299, e-mail: postek@nist.gov
Dr. John A. Dagata, phone: (301) 975-3597, e-mail: john.postek@nist.gov

---

[1]Postek, M. T. 1997. The potentials for inspection and metrology of MEMS using a combined scanning electron microscope (SEM) and proximal probe microscope (PPM). Proceedings SPIE 3225:92-101 (Invited Paper).

[2]Postek, M. T. and Ho, H. 1997. Dimensional metrology at the nanometer level: combined SEM and AFM. Proceedings SPIE 3050: 250-263.

Nanometer Scale Dimensional Metrology With Atomic Force Microscopy

Atomic force microscopes (AFMs), which are capable of nanometer resolution, have emerged as important new instruments for semiconductor applications. Among the potential advantages of AFMs are the ability to image features of almost any material and compatibility with the clean room environment. Presently, NIST has a two-element program to extend the technical understanding of AFM and facilitate the application of AFMs in the semiconductor industry. These elements are: (1) the development of a metrology AFM and (2) collaboration with industrial users and vendors on metrology applications of commercial instruments.

First, NIST has constructed a calibrated metrology AFM (C-AFM) with three-axis interferometric determination of tip position. This is a research instrument specifically designed to aid development of suitable AFM standards, and is capable of nanometer-scale dimensional measurements, with metrology traceable to the wavelength of light in all three axes. Its pitch, height, and width measurement capabilities have been evaluated and are presently at or near desired performance levels. Pitches ranging up to 20 μm can be measured with uncertainties of approximately 3 nm at sub-micrometer scale and approximately 0.07% at the largest scales. Step heights ranging up to 1 μm can now be measured with uncertainties of approximately 1%. The widths of sub-micrometer near-vertical features can be measured to approximately 30 nm, with uncertainty due mostly to correction for the size of the tip.

Second, the NIST program includes collaborations with industrial users and academic researchers on step height and linewidth metrology. A significant component of this effort involves a collaboration with researchers at the University of Maryland on step height metrology at the sub-nanometer scale. These workers have fabricated silicon samples in UHV with single atomic steps on the surfaces. These types of samples have now been studied by many different investigators, and it is widely believed that these samples have considerable potential as fundamental step height and possibly roughness standards. We have performed C-AFM measurements on many such samples, prepared under a variety of conditions. The repeatability of our measurements of these steps is approximately 0.006 nm. The expected value of the step height, based upon the measured lattice constants of bulk silicon, is about 0.314 nm. Currently, the best estimate of our measured step value is 0.300 nm ± 0.006 nm, where the uncertainty represents repeatability only. Although there is a small dependence of the measured value on the algorithm used to calculate the step height, this dependence is roughly 0.004 nm and does not account for the observed difference. We continue to search for systematic sources of uncertainty in C-AFM measurements at this scale, but we cannot rule out the possibility that the native oxide step height differs from the underlying silicon lattice. During FY 1997, we made plans to distribute samples of this type to interested industrial users for evaluation and intercomparison. More than a dozen companies expressed interest in participating. In late FY 1997, our collaborators prepared another set of samples. During FY 1998 we will evaluate and distribute these samples. Additionally, we expect to begin operating our own fabrication facility for such samples during FY 1998. The other major collaboration of the program is conducted through a Cooperative Research and Development Agreement (CRADA) with an IC manufacturer and utilizes an instrument installed in their fabrication facility. The objective is to demonstrate capability for calibrated linewidth and sidewall angle measurements on a commercial noncontact scanning probe instrument which utilizes a "boot"shaped tip. Evaluation of both commercially available and prototype tip characterization and linewidth artifacts is the major component of this work. A reversal technique for the measurement of sidewall angle and tip size correction for the measurement of linewidth are other major features of the approach taken in this work. In the first phase, comparison between these AFM measurements and cross sectional TEM, good agreement was found with about 20 nm uncertainty in linewidth and a one degree uncertainty in sidewall angle. In the second phase of this effort, six similar samples and a commercial "tip characterizer" were measured on this instrument. The next phase of the effort, planned for FY 1998, will be to measure these samples on the C-AFM, once an improved course sample positioning system is in place on the C-AFM. After this phase, some of the samples will be cross sectioned and measured by TEM. The remaining samples will be used in further round robins with other users of AFMs utilizing both conical and boot shaped tips.

This is a dimensional metrology project, with NTRS references identical to those given for the "Dimensional Metrology at the Nanometer Scale: Combined SEM/PPM" project on page 1.

Contacts: Dr. Ronald G. Dixson, phone: (301) 975-4399, e-mail: ronald.dixson@nist.gov
Dr. Theodore Vorburger, phone: (301) 975-3493, e-mail: theodore.vorburger@nist.gov

Linewidth Correlation

NIST is responsible for providing linewidth SRMs (standard reference materials) and/or calibration services to meet the needs of U.S. industry. Our current linewidth standards are optically based with a total uncertainty of approximately 50 nm 2σ. As device sizes shrink, the semiconductor industry needs to measure sub-micrometer lines with uncertainties of a few nanometers. The magnetic recording and photographic industries have gap width and grain size measurement requirements at approximately the same scale.

Neither NIST nor any other national laboratory presently offers a linewidth measurement service or SRM with this level of accuracy. The reason is related to a fundamental difference between a width measurement and other kinds of dimensional measurements such as pitch or height. Microscopes produce images which are distorted representations of the specimen. In general, the distortion includes an error in the location of an object's edge. For pitch and height measurements, where the distance is between two edges of the same type (i.e., either both right edges or both left edges for a pitch measurement; both top edges for a height measurement), the bias cancels to first order. As a result, accurate knowledge of the bias is not necessary for this kind of measurement. But linewidth measurement is a left edge to right edge distance determination. Instrumental bias does not cancel, but *doubles*. Accordingly, physical linewidth determination with any microscopic technique requires modeling of the probe/sample interaction in order to identify edge locations. A barrier to accurate linewidth determination has been acquisition of models in which we can have the required level of confidence.

Linewidth measurement capabilities at NIST span several techniques, including optical, scanning electron, and scanned probe microcopies for physical linewidth as well as electrical techniques to measure the average width of conducting paths. This project seeks cooperative interactions among practitioners of the various techniques. This cooperation includes information exchange among practitioners of the various methods. It includes model development as well as design and execution of experiments for cross-technique comparison of measurements. These intercomparisons serve as a mechanism for cross-checking models and procedures among the different techniques.

This is a dimensional metrology project, with NTRS references identical to those given for the "Dimensional Metrology at the Nanometer Scale: Combined SEM/PPM" project on page 1.

Contact: Dr. John Villarrubia, phone: (301) 975-3958, e-mail: john.villarrubia@nist.gov

Electrical Linewidth and Overlay Metrology

The NTRS specifies linewidths decreasing to 0.1μm from the present 0.5 micrometers within five years. In addition, the NTRS has identified electrical linewidth or "Electrical CD" as a potential solution for both future CD and overlay calibration (NTRS, Figure 22). Metrology users in the semiconductor industry have asked our assistance in fabricating and certifying the dimensions of linewidth reference materials to support linewidth metrology below 0.5μm. This project has three elements: (1) the design and fabrication of electrically testable reference-materials with properties necessary for linewidth-metrology support to 0.1 μm; (2) establishing and documenting the overall performance and suitability of these samples for use in the calibration of metrology instruments used by semiconductor manufacturers; and (3) application of the technology developed to related applications such as placement, step height, and overlay.

Reference-materials with properties necessary for linewidth-metrology support to 0.1 micrometers have been designed and fabricated with a patented silicon-on-insulator architecture. Samples of SIMOX-based test chips having reference features to 0.25 micrometers were measured electrically at NIST. They were distributed to each of 18 members of an industry consortium for measurements by scanning-electron and atomic force microscopy. The results have shown a substantial decrease in methods divergence compared to measurements made on other types of samples. In 1998, a revised test-chip design will be fabricated with BESOI substrates for distribution to the consortium after electrical testing at NIST.

The application of the technology developed for linewidth reference materials is being evaluated for related applications in IC-wafer fabrication such as placement, step height, and overlay. We have fabricated one wafer-lot with some overlay targets having different inter-layer heights. We have also fabricated a test structure with lines up to 10 cm long on single-crystal material. Their parallelism and straightness is being evaluated by NIST's line-scale interferometer. During 1998, additional tests will be performed on these structures by optical and other means for further evaluation for use in overlay and step-height applications.

This is a dimensional metrology project, with NTRS references identical to those given for the "Dimensional Metrology at the Nanometer Scale: Combined SEM/PPM" project on page 1. Electrical linewidth or "Electrical CD" is mentioned specifically as a potential solution, Figure 22 on page 95.

Contacts: Dr. Michael W. Cresswell, phone: (301) 975-2072, e-mail: michael.cresswell@nist.gov
Mr. Richard A. Allen, phone: (301) 975-5026, e-mail: richard.allen@nist.gov

Optical CD and Overlay Metrology

Tighter tolerances on CD measurements in wafer production place increasing demands on photomask linewidth accuracy and on overlay tolerances. NIST has a comprehensive program to both support and advance the optical techniques needed to make these measurements.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch artifacts in the range of 0.5 μm to 30 μm are currently certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm. These standards are being compared with linewidth measurements in other national standards laboratories.[1] An ultraviolet transmission microscope has been constructed that will replace the green light system. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. Reduced transmission of UV through the chrome and reduced instrument vibration will offer improved linewidth uncertainties.

To meet the future challenges in overlay metrology, a new state-of-the-art reflection mode confocal microscope has been constructed at NIST. This instrument also utilizes a Stewart platform. Three-axis interferometry monitors sample position, and a collimated laser beam monitors stage tilt. The optical resolution is nominally 0.25 μm. A CCD camera and image acquisition electronics enable general use of the instrument in reflection mode on semiconductor samples. The overlay metrology program is investigating and designing a new set of overlay standards. These standards will consist of artifacts which will allow users to align their overlay instrument properly and minimize tool-induced shift. Currently under development is the stepped microcone alignment artifact.[2] In parallel with the development of alignment artifacts and two-dimensional scale calibration standards is a research effort into material and geometry issues to determine the best candidate for a calibrated conventional box-in-box overlay pattern.

Two dimensions of interferometry on the overlay metrology tool are now fully operational with a VXI/VME control system. The system can acquire data in an interferometric mode or in a full CCD array mode. These data can then be analyzed with the Matlab based image analysis and signal processing code developed in-house. Prototype stepped microcone artifacts have been successfully fabricated and measured. Data from various step edges on the microcone have been compared to simulated step edge data using the Metrologia program. This experimental/model comparison has led to a SEMATECH/NIST joint venture to improve the simulation to experiment agreement through a series of computer code improvements and extensive measurements using the overlay tool. A thorough quantitative analysis of the overlay system is currently in progress using industry wafers and NIST SRM artifacts. NIST optical overlay personnel are additionally involved in several industry collaborations with SEMI, SEMATECH, IBM, Hewlett Packard, Digital, KLA, IVS, and several others in the design and development of overlay metrology tool alignment structures and conventional overlay target structures to be calibrated at NIST.

NIST is also developing a magnification standard for optical microscopes (SRM 2800) with certified pitch patterns from 1 cm to 1 μm produced on standard size slides. In addition, NIST has outlined a new technique for measurement of photomask linewidths called Emulated Stepper Aerial Image Measurement.

This is a dimensional metrology project, with NTRS references identical to those given for the "Dimensional Metrology at the Nanometer Scale: Combined SEM/PPM" project on page 1.

Contacts: Dr. James Potzick, phone: (301) 975-3481, e-mail: james.potzick@nist.gov
Dr. Richard Silver, phone: (301) 975-5609, e-mail: richard.silver@nist.gov

---

[1]Potzick, J. and Nunn, J., International comparison of photomask linewidth standards: NPL-NIST, Proceedings SPIE 2725-08: 124-129.

[2]Silver, R. M., Potzick, J., Scire, F., Evans, C., McGlaughlin, M., Kornegay, E. and Larrabee, R., A method to characterize overlay tool misalignments and distortions," Proceedings SPIE 3050: 143-155.

High-Accuracy Two-Dimensional Measurements

The ability to place features accurately in 2D has multiple impacts in the electronics industry. Manufacture of reticles, large high-resolution displays, and circuit boards involve different aspects of the same metrology problem.

The situation regarding this critical capability is unusual in that state-of-the-art commercial measuring machines (such as the Nikon 5I or Leica LMS IPRO) are so accurate that there is no available source of better 2D measurements from which standards can be established. As such, each user's measurements today are traceable only to one particular measuring machine. NIST clearly recognizes the industry-wide exposure inherent in this situation and is developing innovative practical approaches to establish convergence in the absence of a conventional standard.

The NIST linescale interferometer is known to provide the most accurate 1D measurements available in the world. Preliminary work has been carried out on algorithms that will allow the use of this tool on the 2D problem. Multiple passes of linear artifacts with different orientations on the customer's measurement machine will provide a reasonable accuracy check. We have designed and built a 2D (200 mm x 200 mm) measuring machine at our Gaithersburg, MD, facility to test algorithm designs and sensor effects. We are working with two companies through the SBIR program to design, implement, and test new algorithms. One algorithm has been implemented and is currently being tested with data from our machine.

In a parallel effort, we are also working with other NIST researchers to involve industry in a suitable interlaboratory test (round-robin) to assess the current industry capabilities.

A larger range machine (750 mm x 750 mm) has been brought on line to make measurements on large grid plates used in PC board and flat-panel display fabrication. The uncertainty (k=2) of measurements on this instrument is 0.4 mm over the full range of the machine.

Two-dimensional measurements are implicitly needed for controlling overlay capabilities of steppers and mask-making tools. Overlay is listed in Table 23, page 83 of the 1997 edition of NTRS as a difficult challenge for both >100 nm and <100 nm processes and states that overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 100 nm. Also overlay over large field sizes will continue to be a major concern for sub-130 nm lithography. It also shows, in Table 26, page 87, that two-point placement accuracy is and will be a critical issue for rules at 180 nm and less.

Contacts: Dr. Ted Doiron, phone: (301) 975-3472, e-mail: theodore.doiron@nist.gov
Dr. Martin Schroeck, phone: (301) 975-4160, e-mail: martin.schroeck@nist.gov

Radiometric Metrology for Deep Ultraviolet Lithography

The *National Technology Roadmap for Semiconductors* identifies improvements in photolithography technology as a critical requirement for shrinking IC feature sizes below the present 250 nm generation. Two key issues are the tightening of photolithography exposure control and the extension to shorter wavelengths. The tightening of exposure control requires improved measurement of absolute dose and uniformity at the wafer. We are addressing this issue by investigating new stable UV source and detector standards, and developing more accurate radiometric scales. Extension of photolithography exposure wavelengths from the present-generation 248 nm to 193 nm and 157 nm requires accurate measurements of the optical properties of the materials to be used as the optical elements of the photolithographic steppers at these shorter wavelengths. We are making accurate measurements of the refraction indices and their thermal coefficients at these wavelengths of fused silica and calcium fluoride, and investigating materials issues such as strain and exposure damage that affect these properties.

The program elements include:

1. Source Standards - The NIST Synchrotron UV Radiation Facility (SURF II) acts as the primary standard for both sources and detectors in the DUV spectral region. An upgrade project (SURF III), to be completed in August 1998, includes an increase in electron energy to allow useful emission of radiation down to 2 nm, an enhancement in absolute current determination, and the addition of two new radiometric beamlines. This facility will achieve a 0.1% standard uncertainty of UV irradiance from 3 nm to 400 nm, and will enable accurate, direct radiance, and irradiance comparisons with new as well as existing source transfer standards.

2. Detector Calibrations - A new radiometric facility has been constructed at SURF II which combines a high-throughput normal incidence monochromator with an absolute cryogenic radiometer to provide absolute detector-based radiometric calibrations in the spectral range from 125 nm to 320 nm. A wide variety of detectors have been characterized, e.g., Si-based diodes, PtSi, GaN and diamond. The facility has also been used to measure the degradation in the diodes induced by exposure to UV radiation. Efforts are underway to construct a separate facility capable of characterizing degradation in diodes to 193 nm excimer radiation.

3. Index Measurements - Collaborating with MIT Lincoln Laboratory on a SEMATECH sponsored 193 nm stepper demonstration project, we have used a goniometric refractometer to measure the refraction index near 193 nm (with an accuracy of 7 ppm), as well as the dispersion and temperature dependence, for several grades of fused silica and calcium fluoride. These measurements are needed for the design of the stepper optics. We plan to continue these measurements on new grades of fused silica and calcium fluoride near 193 nm and, with instrument modifications, on calcium fluoride near 157 nm. We have also designed and begun building a refractometer, based on a DUV Fourier transform spectrometer, capable of an improved accuracy of 1 ppm. The system should be operational by September 1998.

4. Index Issues - Compaction, bulk strain, and impurities in available grades of fused silica and calcium fluoride present problems limiting their suitability for use as optics at 193 nm and below. Our measurements of fused silica have revealed index differences between grades due to these defects. We have also identified significant strain-induced birefringence in candidate grades of calcium fluoride. We are developing optical strain measuring techniques to investigate and quantify compaction and growth strain in fused silica and calcium fluoride, and will work with suppliers to ameliorate these problems.

The expectation that 193 nm lithographic systems will be primary patterning tools for the 180 nm and possibly down to the 100 nm generations is discussed in the Lithography Section of the 1997 NTRS, and summarized in Figure 18 on page 89. Improved radiometric and optical materials metrology are needed for the development of 193 nm systems in order to meet the requirements detailed in Table 24 on page 85.

Contact: Dr. James R. Roberts, phone: (301) 975-3225, e-mail: james.roberts@nist.gov

Deep Ultraviolet (DUV) Laser Metrology for Semiconductor Photolithography

Since the first edition of the *National Technology Roadmap for Semiconductors* (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a shift towards shorter laser wavelengths in the optical lithography process. It is clear that DUV lasers, specifically KrF (248 nm) and ArF (193 nm) excimer lasers, will be the preferred sources for high resolution lithography systems until the future shift to non-optical lithography for the fabrication of devices with feature sizes smaller than 100 nm. To meet the challenge of providing metrology for DUV lasers, the NIST Optoelectronics Division will develop: (1) electrically calibrated DUV laser calorimeters to be used as national primary standards for laser energy measurements, (2) transfer standards to improve the accuracy of measurements at the factory floor, and (3) calibration capabilities for DUV dose (i.e., energy density) measurements.

Several years ago NIST (with the support of SEMATECH) developed primary standard laser calorimeters for 248 nm excimer laser measurements. As a result, NIST now provides laser power and energy measurement services to the semiconductor community at 248 nm with 1 to 2% uncertainties. In addition to the existing measurement services, there is increasing demand for laser dose measurements. Accurate measurements of laser dose are especially crucial to the development of new mask and resist materials at 248 and 193 nm.

Our efforts are now focused on developing the 193 nm measurement capability as quickly as possible and, to this end, are developing (with SEMATECH support) a primary standard laser calorimeter system for 193 nm. Improved transfer standards are needed to assure accurate dissemination of the measurements to industry and to facilitate accuracy improvement activities, such as intercomparisons with calibration laboratories and industry round robins.

The primary objectives of the project are as follows:

1. Develop a calibration facility for 193 nm excimer laser energy and dose meters (including the extension of our current 248 nm service to accommodate dose meters).

2. Develop energy and dose transfer standards appropriate for calibration transfers and accuracy improvement in the semiconductor industry.

According to the 1997 NTRS, optical lithography using 193 nm technology may be viable through 2005, Table 18 on page 89, and non-optical technologies will be available after that to extend beyond the 100 nm generation. NIST is participating in the SEMATECH and MIT Lincoln Laboratory collaboration project on 193 nm photolithography in an effort to provide needed critical data and measurement support as quickly as possible. One critical requirement that has been identified by both MIT Lincoln Laboratory and SEMATECH is the availability of calibration services for 193 nm laser energy meters by June 1998. This requires the development of a 193 nm primary standard, a calibration facility, and appropriate transfer standards to transfer calibrations to the industry customers. Furthermore, the 1997 NTRS has identified the need for more process control in the wafer plane, Table 22 on page 74. This requirement anticipates the need for improved laser dose metrology which can only be accomplished through the development of highly accurate primary standards, transfer standards having both high stability and radiometric accuracy, and a calibration facility to provide the means to calibrate these transfer standards and customer-supplied laser detectors.

Contacts: Mr. Tom Scott, phone: (303) 497-3651, e-mail: scott@boulder.nist.gov
Dr. Chris Cromer, phone: (303) 497-5620, e-mail: cromer@boulder.nist.gov

PROCESSING

Fundamental Process Control Metrology for Gases

Gas pressure, composition, and flow are fundamental operating variables in many semiconductor fab processes. NIST efforts in this important area have a dual focus: first, to ensure that the technical underpinnings of the measurements (including standards and calibration procedures) are available and widely disseminated; and second, NIST is examining the performance characteristics of process monitoring and control equipment to permit their optimum use by the industry.

Real-time monitoring of contaminants and gas composition in a process chamber also requires reliable process monitoring equipment. Preliminary NIST studies of commercial residual gas analyzers (RGAs) found undesirable performance characteristics in most instruments. Results from recent experimental studies on commercial RGAs indicate that most instruments can be optimized to minimize nonlinearities with pressure and "total pressure effects" upon the measured partial pressures of contaminant gases. The experimental data are in qualitative agreement with a theoretical model which ascribes high pressure nonlinearities to electron and ion space charge effects in the ionizer, focusing electrode area, and in the mass filter. The experimental data and model indicate that nonlinearities can be minimized through the appropriate selection of ionizer potential settings.[1] To date, the investigation of RGAs has been limited to those with an open ion source which have maximum operating pressures of 0.1 Pa. Evaluation of RGAs which operate at higher pressures, such as closed ion source RGAs and/or differentially pumped RGAs is now on-going. Testing of the optimization techniques with RGAs on a semiconductor tool in collaboration with researchers at the University of Maryland is planned for the next year.

Responding to the SEMI/SEMATECH Thermal Mass Flow Meter Working Group, NIST has extended flow measurement support for the semiconductor industry by development of new primary flow standards at NIST with uncertainties less than 0.1% and by transferring this measurement capability to mass flow controller manufacturers by way of flow proficiency tests. NIST-designed ultra-stable laminar flowmeter transfer standards,[2] covering a range of 7×10^{-8} moles/s to 7×10^{-4} moles/s with a demonstrated long-term repeatability of 0.1%, have been used to perform on-site proficiency tests[3] at 15 mass flow controller manufacturer calibration facilities. An in-situ primary flow calibration system will be implemented in the coming year for in-line calibration of mass flow controllers on a semiconductor process tool. Acoustic flowmetering techniques are being explored for use as a calibration device for toxic and/or corrosive gases.

Residual gas analysis (gas contaminant monitoring) is mentioned in the 1997 NTRS on page 184. Fluid purity and residual matter in vacuum are discussed on page 177 and in Figure 46. Process control in relation to process sensors, such as partial pressure measurements and flow, are discussed on pages 183 and 184. Key impurity levels in gases range down to a volume fraction of 10^{-11} (10 ppt) by the year 2007.

Contacts: Mr. Stuart A. Tison, phone: (301) 975-2857, e-mail: stuart.tison@nist.gov
Dr. Charles R. Tilford, phone: (301) 975-4828, e-mail: charles.tilford@nist.gov

---

[1]Tilford, C.R., Optimizing Residual Gas Analyzers for Process Monitoring, Proceedings of the Symposium on Process Control, Diagnostics, and Modeling in Semiconductor Manufacturing, Ed. by M. Meyyappan, D.J. Economou, and S.W. Butler, The Electrochemical Society, vol. PV 97-7, pp. 184 (1997).

[2]Tison, S.A. and Berndt, L., High-Differential-Pressure Laminar Flowmeter, Proc. of the 1997 ASME Fluids Engineering Summer Meeting, FEDSM97-3207 (1997).

[3]Tison, S.A. and Doty, S.W., Low-Gas-Flow Proficiency Testing, Proceedings of the 1997 National Conference of Standards Laboratories (NCSL) annual meeting, NCSL, Boulder, CO, pp. 55 (1997).

Low Concentration Humidity Standards

Quantification of the effects of residual water vapor on semiconductor fabrication processes is seriously compromised by large uncertainties in the measurement of humidity levels at or below ≈1000 nmol/mol. Regrettably, standards-grade standards for measurements in this range do not currently exist. This project is driven by the need to establish absolute humidity standards at trace levels, thus enabling the realization of sensitive yet accurate hygrometer technology.

In FY 97, construction of the precision low frost-point humidity generator (LFPG) was completed, and tests were done characterizing its performance. It was demonstrated that the LFPG has a temperature stability of better than ±2.5 mK, corresponding to fluctuations in LFPG mean output of less than ±0.05 %. Plans for FY 1998 include a continuation of experiments designed to assess the overall uncertainty in the generated output. An uncertainty analysis will be completed, and efforts to commission the LFPG as a calibration service will be initiated.

A diode-laser-based hygrometer, custom-designed for monitoring nmol/mol levels of water vapor in gas streams, was used to measure the LFPG output. The hygrometer exhibited relatively fast response (time scales ≤1 min), excellent linearity, and a stability of better than 0.25 %. Furthermore, changes in the LFPG output water vapor mole fraction as small as 0.2 nmol/mol were detectable.

In FY 1997, the development of Cavity Ring-Down Spectroscopy (CRDS) as an absolute technique for measuring species-specific gas phase concentrations continued. Using a novel approach, it was demonstrated that absorption cross-sections can be accurately measured with CRDS. For FY 1998, this approach will be refined and extended to the measurement of trace levels of water vapor. Also, a new CRDS system based on diode laser technology will be designed and constructed, with the intention of measuring water vapor in process gas streams such as phosphine and similar gases that are used in the epitaxial growth of semiconductors.

This is a sensor metrology project, with NTRS requirement identical to those given for the "Fundamental Process Control Metrology for Gases," project on page 9.

Contacts: Dr. Joseph T. Hodges, phone: (301) 975-2605, e-mail: jhodges@nist.gov
Mr. Gregory E. Scace, phone: (301) 975-2626, e-mail: gregory.scace@nist.gov

Plasma and CVD Process Measurements

Improved characterization and control of etching and deposition plasmas are required for the next generation of semiconductor fab processes. NIST is addressing the metrology-related aspects of this problem through development of diagnostic tools and techniques on a simple yet highly-relevant reference platform. These tools probe the microscopic characteristics of the discharge, such as species densities, electron and ion energies, and optical emission characteristics.

While these parameters are the most appropriate to describe plasma conditions, macroscopic parameters (power, pressure, gas flow) are used as control parameters today because the complex relationships among the microscopic variables are uncharacterized. A major task is the development of methods to translate microscopic plasma parameters into macroscopic control parameters.

Much of this work uses a universal plasma reactor called the GEC rf Reference Cell (GEC from the Gaseous Electronics Conference where the idea was conceived). More than 25 such cells are currently in use as a standard, reproducible platform for accurate intercomparisons of experimental data and results from plasma models. The GEC cells at NIST are equipped with a wide range of diagnostics including RF current and waveform analysis, Langmuir probes, optical emission, mass spectrometry with ion energy analysis, 1-D and 2-D laser-induced fluorescence (LIF), and spectroscopic ellipsometry.

To date, these diagnostics have been applied to plasmas of Ar, He, Ne, Xe, Kr, O_2 H_2, N_2, SF_6, CF_4, CHF_3, Cl_2, BCl_3, NF_3, C_2F_6 and various mixtures of these gases. Results have identified diagnostics applicable to industrial reactors and the limits of those techniques, as well as the generation of basic plasma data suitable for the validation of various discharge models.

Examples of specific results include: (1) a complete electrical characterization of the GEC cell, for both capacitive and inductive sources, resulting in improved plasma reproducibility; a provisional patent for a non-invasive, non-perturbing technique for measuring the ion current at wafers exposed to high-density plasmas, based upon electrical measurements; and development of a uniformity and reproducibility monitor for industrial reactors utilizing optical emission measurements; (2) determination of neutral and ionic species in Cl_2-containing plasmas, including measurement of the degree of gas dissociation for different plasma conditions in inductively coupled plasmas; (3) measurement of CF_2 2-D spatial densities in CF_4, C_2F_6, and CHF_3 chamber cleaning and etching plasmas for investigation of plasma uniformity and model validation; (4) development of a database of fundamental electron-interaction data for plasma processing gases; and (5) development of a plasma oscillating probe for the measurement of the electron density in inductively coupled plasmas.

Several related projects supply basic support for modeling electric discharges used in semiconductor fabrication. These include modeling of particle formation in plasma-enhanced and thermal CVD reactors, measurement and analysis of fundamental reference data for industrially-relevant gases, and dissemination of experimental results to more than 20 different laboratories using GEC cells. Recently a WWW page was activated at NIST (http://physics.nist.gov/rfcell) that contains a bibliography of over 100 papers directly related to research performed on the GEC cell, along with other critical information about the reference cell.

Future plans include: (1) development of a new reference reactor more closely resembling industrial designs; (2) development of additional sensors for plasma process monitoring and control, including ion energy sensors; (3) continued measurement, assessment, and distribution (via Internet) of fundamental data for plasma processing gases (Cl_2 and argon) necessary to model commercial reactors and processes; (4) further investigation of uniformity, damage and effluents in chamber-cleaning plasmas; and (5) development of IR and millimeter wave absorption spectroscopy for process control.

The degree of empiricism embodied in the plasma tools of today is so well-known that it almost escapes mention in the 1997 NTRS. For example, the needs for modeling and simulation are presented in Table 28, page 94, and the need for additional process control is presented in Table 30, page 97. The need to narrow process-induced parameter distribution is mentioned on page 61. Needs for modeling for process control for gate dielectrics are discussed on page 80. Gate etch potential solutions are listed in Figure 16, page 75, and doping potential solutions are listed in Figure 17, page 76. Etch potential solutions are discussed on page 105 and listed in Figure 25, page 106.

Contact: Dr. James K. Olthoff, phone: (301) 975-2431, e-mail: james.olthoff@nist.gov

Metrology for Contamination-Free Manufacturing

NIST is addressing chemistry and particle formation/growth/transport in thermal reactors in order to develop microcontamination standards. Improvements in the currently limited understanding of the physical/chemical mechanisms responsible for the formation, transport, and growth of particles in the gas phase are critical for the minimization of microcontaminants in these process reactors. The effort being undertaken here utilizes both measurement and modeling techniques in order to gain an understanding of these physical and chemical particle growth mechanisms. Model validation through coordinated experimentation in prototypical reactors and techniques for collating and disseminating reference data in an efficient and timely manner are both important components of this task.

A rotating disk CVD reactor for laboratory experimentation has been designed and built. The actual laboratory installation of this reactor commenced during FY 1997. This apparatus is capable of achieving a substrate temperature of 1300 K and a rotation rate of 1000 rpm. It will be possible to perform silicon chemical vapor deposition at the purity and cleanliness levels required for microelectronics fabrication. During FY 1998, temperature measurements will be performed both in the gas-phase and on the surface of the rotating disk. Instrumentation will be installed to allow for *in situ* spatially resolved optical measurements of gas-phase species and particle fields in the reactor during FY 1999.

A rotating disk reactor model that predicts the formation and transport of microcontaminants has been developed and awaits experimental validation. This validation will be initiated during FY 1998 with comparisons between temperature profiles calculated numerically and profiles obtained experimentally in the rotating disk reactor apparatus. These comparisons will give a good indication of how well the model is resolving the thermal boundary layer above the rotating disk. This is the critical region for particle formation and growth leading to possible substrate contamination. Additionally during FY 1997, particle contaminant models were developed for the generic plug flow and perfectly-stirred reactor configurations to further aid in the study of particle behavior in actual process reactor systems. These models account for the formation of particles and their subsequent growth via coagulation by means of a moment transport formulation that employs a lognormal distribution function. The results from these models can be utilized to estimate the behavior of actual reactor systems that exhibit characteristics in the range between the two generic cases being simulated.

The effort in the area of physical/chemical properties data for species of importance in semiconductor processing continued during FY 1997 with the addition of the properties of Si_1 and Si_2 silicon hydrides to our Web site (CKMech). During FY 1998, it is planned to assemble a working reaction-set or mechanism for silicon hydride oxidation, which is currently poorly understood. Data will also be made available for silicon oxy-hydrides. These data sets will be made accessible via our Web site or through archival publications.

The need for basic chemical/physical data for equipment modeling, as well as the need for model validation, are discussed in the Modeling & Simulation Section of the 1997 NTRS on page 189. The requirement for contaminant control strategies is discussed throughout the Defect Reduction Section, pages 163 through 178. Table 54 on page 164 calls for advanced chemistry/contamination models for developing defect-free, intelligent equipment. Critical particle sizes for wafer environments are defined in Table 59 on page 170. The need for a more fundamental understanding of reactor contaminant formation/transport is discussed under Process Equipment on pages 177 and 178.

Contacts: Dr. Ronald W. Davis, (301) 975-2739, e-mail: rwdavis@nist.gov
Dr. Donald R. Burgess, (301) 975-2614, e-mail: dburgess@nist.gov

Highly Accurate Thermometry for Semiconductor Processing Using Pure Element Thermocouples

This project focuses on the development of optimal fabrication techniques and maintenance procedures for platinum versus palladium (Pt/Pd) thermocouples and on the determination of a highly accurate emf-temperature reference function for these thermocouples.

The program accomplishments include: (1) An emf-temperature reference function over the range 0 °C to 1500 °C was developed in a joint project between NIST and IMGC. The range of temperature of this reference function is greater than any existing function, and the uncertainty of the reference function is 11 m°C over the range 0 °C to 1050 °C, which is a factor of three to eight less than the uncertainties of existing reference functions; and (2) Pt/Pd thermocouples have been delivered for evaluation to a large industrial supplier of thermocouples for the semiconductor industry. A member of the NIST staff has visited this company to foster development of industrial expertise in the use of Pt/Pd thermocouples.

For FY98, the key elements of the project are: (1) publication in an archival journal of a complete description of the emf-temperature reference function determined by NIST and IMGC; and (2) continued interaction with industrial collaborators, exploring the performance of Pt/Pd thermocouples in diffusion furnace environments.

The need to narrow process-induced parameter distribution is mentioned on page 61 of the 1997 NTRS. The need to reduce thermal budget in processes, and the implication of narrowing the uncertainty in thermal budget, is mentioned repeatedly, pages 59, 72, 73, and 187.

Contact: Dr. Dean Ripple, phone: (301) 975-4801, e-mail: dean.ripple@nist.gov

Temperature Measurement for Rapid Thermal Processing

Achieving accurate temperature measurement in rapid thermal processing (RTP) is crucial to quality control for front-end processing of silicon wafers. The goal of this inter-laboratory collaboration between NIST's Physics Laboratory and the Chemical Sciences and Technology Laboratory is to achieve ±2 °C accuracy and ±0.25 °C repeatability in radiometric temperature measurements of silicon wafers in the RTP environment. This project consists of four major elements: (1) radiometer in-situ calibration using thin-film thermocouples; (2) characterization of new generation radiation thermometers; (3) characterization of wafer radiation environment; and (4) establishing industry collaboration and community support for this project.

The first task of this project is to provide an in-situ, 200 mm silicon calibration wafer instrumented with thin-film thermocouples, so that the radiation pyrometers can be used in wafer processing with temperature uncertainties of less than 2 °C. We are developing and evaluating a calibration methodology to replace the wire thermocouples of current calibration wafers with thin-film thermocouples. The approach will reduce the uncertainty in present wafer technology by (1) reducing the perturbation due to heat transfer at the massive thermocouple junctions in the present technology; and (2) replacing the commercial thermocouples with the superior Pt/Pd system. The approach has three key areas of activity: (1) fabrication and evaluation of 200 mm calibration wafers with the thin-film Rh/Pt and Pt/Pd thermocouple arrays; (2) materials analysis and characterization of Rh/Pt and Pt/Pd thin-film thermocouple systems on silicon wafers using SEM, SIMS, ESCA, and EDX; and (3) high temperature research up to 1300 K using other materials such as W and Re.

Characterization of radiometers includes both calibration and examination for various radiometer performance criteria. Through two CRADAs, calibration procedures for optical fiber and spot type radiometers will be investigated. Additional university grants will assist in the modeling and evaluation of radiometer calibration systems. In all calibrations, a thorough uncertainty analysis will be performed to achieve traceability to the International Temperature Scale of 1990. In addition to calibration, the radiometers will be characterized for uniformity, repeatability, linearity, systematic drift, and other important parameters.

Modeling efforts will be divided into two parts. First, modeling of radiation from the lamps to the wafer will be investigated to try to understand the effects of the source and the chamber on the irradiation to the wafer. Second, modeling of the radiation paths to the radiometer will provide information on how much of the total radiation enters the detector system. This information can be collectively used in future experimental designs, understanding of the heat transfer phenomena, and resolution of measurement and calibration problems.

Industry collaboration with NIST in this project is crucial and is evident with the CRADAs and university grants that have been mentioned. With over 40 participants, the second annual RTP Advisory Group Meeting was held at NIST in January to present the status of the NIST RTP project and to gather input on issues of interest to the RTP community. Suggestions from this meeting are being considered and will result in a summary report to be distributed to each workshop participant.

The ±2 °C uncertainty requirement in temperature measurements for RTP tools was established by the Technical Working Group on Manufacturing of the 1997 NTRS and is derived from the 1999 requirement for 0.18 μm linewidths. Both the ±2 °C accuracy and ±0.25 °C repeatability requirements have been quoted from Don Lindholm's keynote address at the RTP '97 Conference. RTP is a key technology for the cluster tool, single wafer manufacturing approach that will be needed to produce ASICs and DRAMs with reduced linewidths and thermal budgets.

Contacts: Dr. Benjamin K. Tsai, phone: (301) 975-2347, e-mail: benjamin.tsai@nist.gov
Dr. David P. DeWitt, phone: (301) 975-4199, e-mail: david.dewitt@nist.gov
Dr. Kenneth G. Kreider, phone: (301) 975-2619, e-mail: kkreider@nist.gov
Dr. Christopher W. Meyer, phone: (301) 975-4825, e-mail: cmeyer@nist.gov

Particle Measurements in Support of the Semiconductor Industry

The project objective is to develop a facility for accurately measuring particle size/concentration and for depositing monosize particles on calibration artifacts to support the *National Technology Roadmap for Semiconductors* goal of quantifying 75 nm diameter particles by 2001. The focus during the past year include: (1) uncertainty assessment of 100 nm SRM®; (2) hardware and modeling advances for the differential mobility analyzer (DMA); and (3) size distribution measurements in support of CRADA with Duke Scientific Corporation.

The project's accomplishments include:

1. The NIST 100 nm SRM® is a critical metrology standard for scanning surface inspection systems. A reanalysis of the measurement uncertainty has resulted in a factor of two reduction in the expanded uncertainty to a value of about 1 nm. The major reasons for the reduction are the new guidelines for evaluating uncertainty (NIST Technical Note 1297) and recent measurements of the Cunningham slip correction. It was found that the JSR Company's 100 nm calibration particles were 10% larger than the NIST particles. This finding has important implications, because the JSR Company particles have been used in assessing the minimum size detected by some wafer scanner manufacturers.

2. An improved DMA inlet was developed in collaboration with Drs. Pui and Chen at the University of Minnesota. By reducing the aerosol inlet gap from about 9 mm to 0.8 mm, it was possible to measure the CV (0.02) of the 100 nm SRM particles with essentially no instrument broadening. There was evidence of flow recirculation and field penetration when using the old inlet for these conditions. A second collaboration involved Monte Carlo simulation of the diffusional loss of the particle in the DMA with Dr. Hagwood from Statistical Engineering at NIST and Dr. Sivathanu from Purdue. This is the first analysis including wall loss of the diffusing particles and leads to a correlation for the effect of diffusion on the broadening of the instrument response.

3. In April of 1997, NIST entered a CRADA with Duke Scientific Corporation on the measurement of monosize polymer microspheres less than 125 nm diameter. NIST is interested in the size range 30 nm to 125 nm to support the NTRS concerning particle contamination on wafers. During the past year NIST has measured the size distribution of 18 polymer samples with mean sizes ranging from 70 nm to 105 nm using a high resolution DMA. Duke Scientific has been able to better adjust the polymerization parameters as a result of the NIST size distribution measurements. The end result is a significant reduction in the width of the size distribution.

These studies have led to three manuscripts; a fourth manuscript on the measurement of three calibration particle sizes (92 nm, 127 nm, and 218 nm) will be prepared for the upcoming International Conference on Characterization and Metrology for ULSI Technology to be held at NIST in March. Work is in progress to characterize a nominal 75 nm calibration particle size. In collaboration with the University of Minnesota and TSI Inc., the feasibility of using electrospray for aerosolizing polystyrene spheres from 90 nm to 30 nm will be evaluated. Electrospray produces droplets about a factor of 10 smaller than conventional pneumatic atomization, thus resulting in a smaller residue layer from the water.

Particle contamination appears throughout the Crosscutting Working Group on Defect Reduction in the 1997 NTRS. Table 57 page 167 indicates that improvements are needed starting year 1999 for both patterned and unpatterned wafer defect detection to stay with the NTRS Roadmap. Currently, there is no known solution for the 2006 goals regarding defect detection.

Contacts: Dr. George W. Mulholland, (301) 975-6695, e-mail: george.mulholland@nist.gov
Dr. William Pitts, (301) 975-6486, e-mail: william.pitts@nist.gov

Optical Scattering for Wafer Surface Metrology

Optical scattering tools are indispensable in modern fabrication lines for sizing and counting defects and particles. As feature sizes decrease and aspect ratios increase, the requirements for the detection of defects and contamination become tighter. This program focuses on developing a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, and characterize the response of instrumentation to different types of defects.

The bidirectional reflectance distribution function (BRDF) quantifies the directional dependence of light scattering. The Goniometric Optical Scatter Instrument (GOSI) at NIST features a wide dynamic range, high angular accuracy, very low instrumentation scatter contributions, multiple incident wavelengths (visible and UV), and polarization control on both the incident and viewing light. GOSI is capable of measuring the polarized BRDF for nearly any two incident/viewing directions and is useful as a tool for calibrating angle-resolving and angle-integrating optical scatter instrumentation and well as a tool for research.

A second instrument, the Scanning Optical Scatter Instrument (SOSI), is under development to complement the capabilities of GOSI. An instrument with 28 fixed detection elements covering the scattering hemisphere, it will enable high-speed determination of the polarized BRDF, or the differential scattering cross section, at any location on a wafer surface. Together with an understanding of the light scattering functions for different types of sources, SOSI will have a substantially improved capability for detecting and identifying defects, particles, and microroughness on a wafer surface.

Near-term work is aimed at:

1. Developing methodologies for characterizing commercial scanning surface inspection systems. Recently, a software package was developed that can be used to estimate the response function of an instrument to surface microroughness. Intercomparisons between fabrication line instruments are being organized to validate this methodology.

2. Exploring bidirectional ellipsometry as a tool for identifying defects on silicon wafers, wafers with blanket dielectric or metallic layers, and patterned wafers. Since the polarization of light is very sensitive to the source of optical scatter, this technique enables discrimination between a variety of defect types.

3. Measuring the BRDF from particles on bare silicon wafers. This research will enable algorithms to allow scanning surface inspection systems to determine particle size and composition, and allows the testing of theoretical models for light scatter.

Defect detection plays an important role in maintaining high production yields on fabrication lines. Defect detection needs are mentioned throughout the 1997 NTRS, with specific detection requirements outlined in Table 57 on page 167.

Contact: Dr. Thomas Germer, phone: (301) 975-2876, e-mail: thomas.germer@nist.gov

High-Resolution X-Ray Spectrometer for Chemical Analysis

Improved X-ray detector technology for materials analysis has been cited by SEMATECH as one of the most important metrology needs for the semiconductor industry. The transition-edge sensor (TES) microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive (EDS) detectors. One of the most critical analytical needs, as specified in the Metrology Supplement to the *National Technology Roadmap for Semiconductors* (NTRS), is the identification and chemical analysis of small particles and defects, for which current X-ray microanalysis methods fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. The current generation of TES microcalorimeters has already demonstrated identification of 0.2 μm particles and observation of chemical shifts in elemental spectra. It is anticipated that the TES microcalorimeter will be able to meet both the near-term (1998 to 2000) NTRS goal of identifying particles as small as 0.08 μm in diameter and the longer-term requirements of the semiconductor industry for improved particle identification and analysis.

The performance of the TES microcalorimeter was improved significantly in 1997. The resolution of the instrument, which was already over an order of magnitude better than conventional semiconductor EDS detectors, was improved by another factor of 2, to 3 electron volts. At the same time the speed of the detector, as measured by X-ray count rate, was also increased by nearly a factor of 2, to 450 cps. The collection area of the detector was increased (to 4 mm^2 effective area) with the use of an X-ray polycapillary optic lens and now approaches that of semiconductor EDS detectors. This TES microcalorimeter allows straightforward identification of closely spaced X-ray peaks in complicated spectra, including the severe peak overlaps in important materials (such as TiN and WSi_2) which cannot be resolved by semiconductor EDS detectors. It is clear, however, that the fundamental limits of this type of detector have not yet been reached. In the next year it is anticipated that both energy resolution and speed can be improved through development of new fabrication methods for the detectors. Further engineering is also needed to improve the stability of the system against changes in SEM operating conditions.

The detector has been used to demonstrate particle identification of 0.3 μm W particles on Si substrates. Independent of the small size of these particles, this is a difficult identification problem due to the severe peak overlap between the Si-K and W-M lines, and is not possible with conventional semiconductor EDS detectors. Practical demonstrations of this capability on real samples from industrial collaborators are planned for 1998. With improvements in the entire detector system (both SEM and spectrometer), it is anticipated that the NTRS goal of identifying 0.08 μm particles should be achievable in the near future.

The improved energy resolution of the detector achieved in 1997 has enabled the use of the spectrometer to observe shifts in the spectra of elements depending on their chemical bonding state. By carefully calibrating the response of the detector, chemical shifts between Al and Al_2O_3 and between Fe and Fe_2O_3 were measured. Because the shift in energy due to chemical bonding is small (on the order of a few electron volts), such observations are impossible with conventional semiconductor EDS detectors. In 1998 the goal will be to demonstrate chemical analysis on small particles, with the Al/Al_2O_3 system being of particular interest to the semiconductor community.

Detailed guidance regarding instrumentation is outside the scope of the 1997 NTRS. However, strong industrial support for this effort has been registered by the SEMATECH Analytical Lab Managers Working Group.

Contacts: Dr. David Wollman, phone: (303) 497-7457, e-mail: wollman@boulder.nist.gov
Dr. John Martinis, phone: (303) 497-3597, e-mail: martinis@boulder.nist.gov
Dr. Gene Hilton, phone: (303) 497-5679, e-mail: hilton@boulder.nist.gov
Dr. Kent Irwin, phone: (303) 497-5911, e-mail: irwin@boulder.nist.gov

Chemical Characterization of Thin Films and Particle Contaminants

Characterization of the elemental composition, crystallographic phase, and chemical structure of microelectronic components and particle contaminants at nanometer spatial resolution is necessary for understanding and improving the performance of advanced devices. NIST is meeting these needs by: (1) developing high resolution Transmission Electron Microscopy (TEM) analysis methods; (2) comparing existing particle analysis methods with new approaches; (3) developing variable angle grazing incidence X-ray photoelectron spectroscopy (GIXPS); and (4) applying the methods to real analytical problems via collaborations with the semiconductor industry.

The TEM allows direct imaging and analysis of the complex interlayered structures composing microelectronic devices. We are applying elemental analysis using Electron Energy Loss Spectrometry (EELS) and X-ray spectrometry combined with near atomic resolution imaging of cross sections to characterize devices. This year we developed and demonstrated electron holographic analysis capabilities on the TEM for the imaging of the electron phase and amplitude. We initiated development of public domain software for the analysis of TEM electron diffraction patterns of thin film semiconductor materials for compound identification and analysis. This work aids the microscopist by improving the diffraction measurement accuracy and precision and removing the tedium.

We developed and demonstrated a telepresence microscopy and microanalysis system that allows us to collaborate with the semiconductor industry live-time over the WWW. Many of our microscope imaging and spectroscopy systems have been wired directly to the world wide web and dramatically improved information transfer to collaborators.

Particle contaminants during device manufacture are a significant source of device failure. Characterization of particle composition allows the fabrication facility to identify and control the particle source. We determined the effect of chemical valence state on X-ray emission analysis using electron beam instruments. This work allows us to understand the quantitation of compound identification using high spatial resolution, low energy X-rays.

GIXPS is used to explore chemical bonding with nanometer spatial resolution. Taking measurements at various grazing angles of the incident X-ray beam allows GIXPS to map the chemical bonding of a device as a function of depth. We are applying this technique to analyze the structure of thin oxide films on silicon devices. A new GIXPS system was installed on our synchrotron beam line at Brookhaven.

Our collaborative effort between NIST and MIT Lincoln Laboratory is continuing to address problems in deep submicrometer CMOS process technology. Advanced processing technologies are being developed for silicon-on-insulator (SOI) CMOS devices by the Lincoln Laboratory group. The multidisciplinary state-of-the-art analytical tools available at NIST are being applied to performance-limiting factors, materials characteristics, and quality of device features.

Electron beam microscopy and characterization needs are discussed in the 1997 NTRS on pages 182, 185, and in Figure 48 on page 185. SOI technology needs are covered in the 1997 NTRS on pages 60 and 62, and in Table 19 on page 60. Thin film metrology needs are covered on page 79 of the 1997 NTRS.

Contact: Mr. Eric Steel, phone: (301) 975-3902, e-mail: eric.steel@nist.gov

FRONT-END PROCESSES

Wafer and Chuck Flatness/Thickness

Limited lithographic depth-of-focus budgets for finer features on larger silicon wafers pose new challenges for flatness and hence for flatness metrology; distortions induced by conventional vacuum chucks are part of the problem. The project has three aspects addressing elements of the problem: (1) interferometric measurement of as-chucked wafer flatness; (2) interferometric measurement of thickness variation; and (3) development of new polishing processes.

NIST has further developed its flat calibration capabilities using a commercial Fizeau interferometer to uncertainties approaching 2 nm over diameters up to 150 mm. The entire wafer is imaged at once, unlike techniques using scanned probes. That image provides a useful qualitative picture of the flatness, while the quantitative description is extracted from on-line analysis of the data. This method has being extended to 300 mm wafers by applying a technique well known to the optics industry (the Ritchey-Common test) but with increased uncertainties. The optical system is in place to allow measurement of as-chucked wafer flatness for 300 mm wafers. The uncertainty for 300 mm apertures will be further reduced with a next-generation interferometer due for installation at NIST in 4Q98.

In a parallel development, the NIST team has developed a new concept for measurement of thickness, free-standing bow, and thickness variations. Wafers will be measured at three positions in a transmission infrared interferometer. The wafer is flipped front to back between two of the observations, allowing bow to be separated from average thickness and mapped independently. Demonstration of principle is completed, and a commercially built instrument based on the principle will be installed at NIST in 1Q98.

NIST capability in flatness measurement will be used to evaluate issues associated with specific vacuum chuck systems as well as to explore new chucking concepts. One important short-term issue is the differing distortions caused by chucks on actual lithography equipment versus those on commercial instruments designed to measure wafer flatness. NIST is developing chucks made of hard, porous ceramics which can be made extremely flat and provide superior support of the wafer from a large number of distributed points; other chuck concepts will be explored.

A novel lap concept has been developed (patent applied for) and applied to both diamond lapping and chemo-mechanical polishing (CMP) processes. Rapid, low-damage lapping of crystalline substrates (silicon, sapphire) has been demonstrated; the potential to reduce wafer fabrication times through combinations of diamond lapping and current processes has been demonstrated. The new lap has been used to polish tungsten, copper, and sheet oxide.

Conversion to 300 mm wafers will peak in 2001-2 (1997 NTRS, page 63) with site flatness (25 x 40 mm) below 100 nm by 2006 (1997 NTRS, Table 20, page 64); development of wafer preparation processes for 300 mm wafers are underway (1997 NTRS, Figure 14 on page 67, and industry contacts) and SOI may become more than a niche technology for 130 nm and beyond (1997 NTRS, page 60). Issues with CMP are discussed in 1997 NTRS pages 106 through 108.

Contacts: Dr. Christopher Evans, phone: (301) 975-3484, e-mail: christopher.evans@nist.gov
Dr. E. Clayton Teague, phone: (301) 975-6600, e-mail: clayton.teague@nist.gov

Measurements and Standards for Thin Dielectric Films

Optical measurement tools for monitoring and control of current and future gate dielectric fabrication processes are required to have precision and resolution smaller than atomic dimensions. Yet as gate dielectrics become thinner, they will become more structured and more difficult to interpret. There is a critical need for reference materials, accurate optical functions of film component layers, and accurate knowledge of layer structure so that optical measurements results will be better predictors of the electrical properties of the films. This project consists of three elements: (1) developing more effective traceability mechanisms for reference materials; (2) developing accurate optical function data at processing temperatures for crystal silicon and critical dielectric films, and (3) improving the understanding of structural properties of gate films through application of a variety of physical and electrical techniques.

Project accomplishments include:

1. Analysis was completed for a comparison study between NIST and a supplier of secondary standards for SiO_2 film thickness conducted to support NIST traceability for films at the 5 nm level for single-wavelength ellipsometry. The experience gained in this testing will be used to design a prototype methodology for a NIST Traceable Reference Material (NTRM) mechanism for additional thin film reference materials. Work will also focus on expanding the reference materials effort to full spectroscopic ellipsometry, and to developing stabilizing or cleaning procedures that will enable reference materials to be maintained with a precision of 0.015 nm. The latter requirement was emphasized by participants in a NIST-sponsored workshop on Thin Dielectric Materials held in October 1997.

2. After extensive performance evaluation and troubleshooting, a custom-built UHV chamber capable of elevated wafer temperatures to 1000 °C and equipped with fast-scanning spectroscopic ellipsometer and RGA is being brought on-line. The unit will be used to generate accurate dielectric function data for substrate silicon and important dielectric films, over a range of elevated temperatures used for film fabrication. The development of these data, which will begin in the second quarter of FY 1998, is expected to improve the utility of in-situ optical monitoring for thin film fabrication processes. Temperature-dependence of the spectral portion of the silicon pseudo-dielectric function in the region of the E_1 interband transition will be analyzed for possible application as a control point for temperature during processing.

3. Collaborations are being developed, both internal and external to NIST, for comparison of diverse measurements of thin dielectric films. Initial results of a comparison of spectroscopic ellipsometry, neutron scattering and X-ray reflectivity on a 10 nm NIST SiO_2 SRM gave agreement on film thickness of about 0.1 nm with a comparable structural model, but showed differing sensitivities of the techniques to surface and interface artifacts. Additional multitechnique evaluations are being developed for thinner films. Previous successful implementation of a two-terminal electrical evaluation, based on a quantum mechanical interference effect, to the buried interface roughness of 0.35 μm n-channel devices is being further extended to other pertinent devices. Capability for state-of-the-art C-V and I-V analysis of gate films is being established. Improved understanding of film structure will be used to develop correct and robust film thickness evaluation by electrical techniques.

Thin film processes and requirements are discussed in the Front End Processes Section of the 1997 NTRS, pages 71, 72, 79, 80, 81, in Table 22 on page 74, and in Figure 16 on page 75. Associated metrology requirements and reference materials are discussed in various sections, pages 50, 79, 80, 178, 181, and 186.

Contact: Dr. James R. Ehrstein, phone: (301) 975-2060, e-mail: james.ehrstein@nist.gov

Scanning Probe Microscopy for Dopant Profiling

NIST is developing the Scanning Capacitance Microscope (SCM) and related software analysis tools with the goal of meeting the NTRS requirements for off-line 2-D doping characterization of 5% precision in dopant concentration and 5 nm spatial resolution. The project has two elements: (1) development of accurate SCM models and theoretical understanding; and (2) improvement of the practical metrology aspects and usability of the tool. The three-dimensional dopant profiles in silicon transistors largely determine the performance and hot-carrier reliability of modern devices. Precise and accurate measurements of 2-D dopant profiles in silicon could be used to calibrate technology computer-aided design (TCAD) simulations of the dopant profile produced by specified fabrication processes.

While SCM images of cross-sectioned transistors containing p-n junctions are now routine, extraction of high confidence 2-D dopant profiles from these images remains elusive. Real devices containing p-n junctions cannot be precisely interpreted with the models developed for dopant gradients in like-type silicon. Extensive Finite Element Method simulations of SCM images including a realistic tip shape across p-n junctions are underway. The work seeks to develop the understanding needed to implement a practical measurement procedure and models to interpret SCM images that contain p-n junctions.

For the SCM technique to meet the NTRS dopant profiling goals, it must be possible to practically convert measured SCM images to 2-D dopant profiles. The NIST SCM models have been integrated into our FASTC2D SCM image-to-dopant profile interpretation software. FASTC2D utilizes a database of calculated SCM capacitance-voltage (C-V) curves to rapidly convert SCM signal to an equivalent dopant concentration. A personal computer-based version of FASTC2D with an intuitive graphical interface and performing at a level to allow rapid interactive extraction of dopant profiles will be completed this year. The NIST SCM technology will be transferred to our industrial partners through distribution of our interpretation software and through cooperative research. To become an accepted tool, SCM must demonstrate its spatial resolution, dopant concentration precision, and reproducibility. Cooperative research projects between NIST and industrial users are essential to develop standard test methods and to demonstrate site-to-site comparability of SCM measurements.

The 1997 NTRS lists 3-D dopant profiling as one of the five most difficult future metrology challenges in Table 28 on page 94, with performance goals listed in Table 29 on page 96. SCM and SPM based techniques for dopant profiling are discussed in the Metrology section, and for overlay measurements in the Lithography section.

Contact: Mr. Joseph J. Kopanski, phone: (301) 975-2089, e-mail: joseph.kopanski@nist.gov

Thin-Film Profile Measurement Methods and Reference Materials

NIST is pursuing a multifaceted analytical approach to 2D and 3D compositional profiling. Main objectives of this work are to: (1) define optimum protocols for ultra-high depth resolution and ultra-shallow profiling by Secondary Ion Mass Spectrometry (SIMS); (2) develop methods to improve the uncertainty of implant dose measurements by SIMS; (3) develop depth-profiling reference materials to assist the semiconductor industry; and (4) develop a quantitative 3-D image-depth-profiling method with submicrometer lateral resolution using SIMS.

For ultra-high depth resolution profiling, we have explored the use of a rotating SIMS sample stage to minimize sputtering-induced roughness as a factor in depth resolution. A large improvement in the profiling of metal multilayers has been demonstrated. We are also studying the use of novel primary ion beam species in commercial SIMS instruments to improve depth resolution. Working with a U.S. instrument manufacturer, NIST is developing a filament-based duoplasmatron ion source to produce molecular ion beams such as SF_5^+ with sufficient beam current to be practical for depth-profiling applications. This species produces much less sub-surface rearrangement of the sputtered sample than does more conventional ion beam species such as O_2^+ or Ar^+. After several iterations of source design, a stable SF_5^+ beam with a current approaching 100 nA has been achieved. We intend to demonstrate the depth resolution achievable with this source during FY 1998.

NIST recently collaborated with Lucent Technologies to study the limits of implant dose measurements that are possible by SIMS. The boron doses of three implants of BF_2 in silicon, in nominal 5% steps, were measured independently by SIMS at the two laboratories, each using carefully designed measurement protocols that incorporated the previously developed NIST SRM 2137 (boron implant in silicon) for dose calibration. Both labs could correctly distinguish the dose order of the three samples; the average dose disagreement between the labs was 1.3%. Further comparisons are planned during FY 1998 to assess the level of agreement that can be achieved for arsenic and phosphorus implants.

The results of a previous round-robin study in which NIST participated provided a strong motivation for NIST to develop an arsenic-implant Standard Reference Material, which has also been designated a priority item by the SEMATECH Analytical Laboratory Managers Working Group. We obtained very uniform As-implanted Si wafers, had them diced into 1 cm square pieces, and measured the As content in representative pieces by neutron activation analysis (NAA), along with two independent solution standards. The NAA results were used to calculate a certified As dose of $7.27 \times 10^{14}/cm^2$, with an expanded uncertainty of $0.077 \times 10^{14}/cm^2$. This material, designated SRM 2134, will be available for sale early in FY 1998. We intend to begin investigating certification methods for a phosphorus implant SRM, and for a depth resolution reference material, in FY 1998.

The need for improved SIMS capabilities for ultrashallow doping profile measurements and offline doping process control is discussed in the 1997 NTRS under Process Integration, Devices, and Structures, page 58, under Front End Processes, page 80, and under Metrology in Table 61 on page 181 and in Figure 48 on page 185. Requirements of reference materials are discussed in general on page 186.

Contacts: Dr. David S. Simons, phone: (301) 975-3903, e-mail: david.simons@nist.gov
Dr. Greg Gillen, phone: (301) 975-2190, e-mail: greg.gillen@nist.gov

Ultra-Thin Dielectric Reliability Metrology

As the semiconductor industry continues to scale device dimensions to achieve channel lengths below 100 nm, gate dielectrics must be scaled to have an equivalent thickness below 2 nm. The reliability of gate oxides is becoming a critical concern as oxide thickness is scaled below 4 nm in advanced CMOS technologies where devices will operate with higher gate electric fields and direct tunneling currents passing through the gate dielectric. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. The project consists of two elements: (1) improved physics and characterization of time-dependent dielectric breakdown of ultra-thin gate oxides and (2) development of highly accelerated dielectric integrity test standards.

Project accomplishments include:

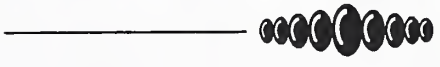
1. New experimental results provide evidence that electrically active defects are not responsible for the wear-out and breakdown of thin gate oxides during constant voltage time-dependent dielectric breakdown (TDDB) tests. Oxide aging during constant voltage stress results from the accumulation of an inactive or latent defect similar to that observed in plasma charging. This new information gives insight into the physical model for dielectric breakdown and has resulted in a new accelerated test that can be used during production to monitor the long-term reliability of ultra-thin gate oxides. The project has perfected the use of high temperatures to accelerate failure so TDDB tests can be performed at lower electric fields closer to operating conditions. These tests will be extended to 3 nm SiO_2 and oxy-nitride films during FY1998. Field acceleration parameters and thermal activation energies that are required for reliability extrapolation and modeling will be determined.

2. Highly accelerated breakdown tests used as production monitors must also be reevaluated for ultra-thin gate oxides. Ramped voltage and current breakdown tests do not work properly for films less than 4 nm. A new voltage ramp technique has been developed through a project coordinated collaboration between JEDEC and ASTM. A round-robin is being planned to evaluate the new test which can be used to evaluate the dielectric integrity of films down to 2 nm. In FY1998 the project will continue its leadership role in the JEDEC and ASTM standards committees to upgrade and modify a current-ramp test standard and develop new standards for monitoring plasma-induced damage and stress-induced leakage current.

Gate dielectric scaling is recognized by the NTRS as one of the five difficult challenges for >100 nm technologies (p. 60, table 19). "Below 180 nm, the key reliability issues will be the quality of very thin gate oxides...." (p. 55). "For thin nitrided oxide a key challenge will be understanding the mechanisms of basic oxide conduction and reliability wear-out failure potential" (p.56).

Contact: Dr. John S. Suehle, phone: (301) 975-2247, e-mail: john.suehle@nist.gov

INTERCONNECT



Interconnect Materials and Reliability Metrology

Thin-film conductors are an essential component of all advanced electronic devices. This project focuses on the two major failure mechanisms of these conductors: electromigration and stress voiding. It develops metrology for reliability evaluation of electrical interconnects, for measuring pertinent mechanical properties of thin metal films, and for understanding the microstructural processes that affect reliability.

Interconnect Reliability

This task develops, evaluates, and refines test structures, test methods, and diagnostic procedures for improving the reliability of metal interconnects and promotes the use of a building-in reliability approach as a cost-effective and rapid means to assure reliability of present and succeeding technology generations. Reliability metrology for Cu interconnects began on four fronts: analysis of published Cu resistivity data for a method to measure electrically the thickness of copper films and the cross-sectional area of copper lines, work with the SEMATECH Cu/lo-k project to evaluate this method experimentally, development of a test-structure design and analysis method for the Cu/lo-k project to measure interconnect linewidth and the magnitude of "dishing" due to chemical-mechanical polishing, and a compilation of best-practice designs for test structures to characterize electromigration (for the SEMATECH RTAB). Reliability test patterns NIST 33 and 34 were designed to evaluate the precision of three electromigration standards and to measure strains in interconnects. NIST 36 is being designed to develop reliability test standards for via structures.

Mechanical Behavior of Interconnect Films

The microscopic laser speckle interferometry technique for displacement measurement on microscale tensile specimens was developed and used to confirm the low Young's modulus values previously seen in Cu thin film specimens. The technique was transferred to several semiconductor industry laboratories, and this technology transfer process will continue. New etching procedures to make the silicon-frame tensile specimens are being developed to make the process more acceptable to industry. The current technique is limited to specimens 20 μm wide and larger. Methods to evaluate samples with widths in the micrometer and sub-micrometer range will be developed and evaluated. One possible approach is use of an alternate actuation method such as an atomic force microscope with a special tip to measure the much smaller forces, of the order of micronewtons. Improved techniques for much smaller specimen preparation will also be required. Collaborations are underway with ITRI, Motorola, Fujitsu, Intel, Dow Corning, and others.

Stress Voiding and Electromigration Studies

Stress voiding test structures were designed and incorporated into the NIST 34 standard test chip. Analysis was performed on 300 backscatter Kikuchi diffraction patterns from narrow Cu conductors which had undergone stress voiding. We observed that grain boundary triple junctions that favor rapid stress void growth may not necessarily favor rapid electromigration void growth. As interconnect linewidths become narrower, *local* heterogeneities in microstructure become the weak links, so microstructure-based studies are under way to explain the selectivity in local failure sites. Anticipated benefits include: (1) accurate data for input into reliability models, (2) full correlations between different processing variables and the results' effect on performance, and (3) development of characterization methods suitable for application to future generation interconnect systems. Collaborations are underway with TexSEM Laboratories, Tosoh SMD, Intel, Cornell University, and the University of Michigan.

Interconnect reliability is at the core of the five most difficult challenges for the industry before 2006 that were identified in the 1997 NTRS, page 99.

Contacts: Dr. Harry Schafft, phone: (301) 975-2234, e-mail: harry.schafft@nist.gov
Dr. David T. Read, phone: (303) 497-3853, e-mail: david.read@nist.gov
Dr. Fred R. Fickett, phone: (303) 497-3785, e-mail: fred.fickett@nist.gov
Dr. Robert R. Keller, phone: (303) 497-7651, e-mail: bob.keller@nist.gov
Dr. Christine E. Kalnas, phone: (303) 497-7496, e-mail: kalnas@boulder.nist.gov

Thin-Film Characterization from Transmission-Line Measurement

This project develops methods to accurately measure the electromagnetic properties of thin films from easy-to-perform in-situ transmission-line measurements. The project brings NIST's Electromagnetic Properties of Materials Group and the NIST MMIC Program into a collaborative effort with IBM to develop microstrip test vehicles, with Texas Instruments to develop coplanar waveguide test vehicles, and with Dow Chemical to investigate NIST-fabricated test vehicles. Planned interactions with SEMATECH will help disseminate the methods.

The methods described below are based on measurements of small printed transmission lines incorporating the materials to be characterized. They allow the dielectric constants of thin films and the conductivities of the metals used in the lines' construction to be determined over broad frequency ranges.

1. **Texas Instruments - The Coplanar Approach.** In a collaborative effort with Texas Instruments, we designed experiments and fabricated and tested coplanar waveguides passivated with BCB, HSQ, and SiO_2 films. The measurements convincingly demonstrate the approach. We have returned the coplanar samples to Texas Instruments for a cross-sectional analysis required to compute the dielectric constants and loss tangents of the thin films from the measured data. In FY 1998 we will complete the analysis and explore its application to Xerogel interlevel dielectrics fabricated at Texas Instruments.

2. **IBM-The Microstrip Approach.** Only a small portion of the electromagnetic energy in coplanar transmission lines is located in the passivation layer we would like to characterize. In a joint effort with IBM we have designed microstrip test structures with greater sensitivity. We completed the layout work with IBM about mid-year. We anticipate receiving our first test structures from IBM in a few months and completing testing in FY 1998.

3. **Dow Chemical Testing Materials Properties.** We are using NIST's unique processing capabilities to pursue a very different approach to dielectric thin-film characterization of materials provided by DOW Chemical, a major supplier of low-κ dielectrics. In our collaboration with Dow we will perform most of the microfabrication at NIST; Dow will simply deposit and pattern the thin films on pretested circuits provided by NIST. A second set of measurements made at NIST will test for the differences in transmission-line capacitance. In FY 1997 we worked with Dow to define responsibilities and completed the test-structure design. In FY 1998 we plan to fabricate samples for and test the methodology.

In the 1997 NTRS, the use of low-κ dielectric appears several times in the Potential Solutions roadmaps on pages 100 to 102. In the Priority of Technology Needs section (for interconnect) on page 103, it states, "It is expected that low dielectric-constant materials will have an even greater impact than low-resistance metals (on performance)." SEMATECH recently indicated to NIST that they ranked the electromagnetic characterization of thin-films a high priority metrology need in the semiconductor industry.

Contacts: Dr. Dylan F. Williams, phone: (303) 497-3138, e-mail: dylan@boulder.nist.gov
Mr. Michael D. Janezic, phone: (303) 497-3656, e-mail: janezic@boulder.nist.gov

PACKAGING

Experimental Micromechanics by e-Beam Moiré

Failure of electronic packaging is a major source of concern in modern electronics. In this project, we seek to improve the usefulness of modeling and simulation in the design and manufacture of advanced electronic packaging and interconnect structures by providing direct quantitative experimental verification of predicted deformations, and by characterizing actual failure modes. To this end, we develop and apply the electron-beam (e-beam) moiré technique to measurement of strain and observation of deformation at high magnification and use the observations to characterize failure modes and to verify mathematical models and simulations of microscale mechanical behavior.

In 1997 we completed thermal loading tests on specimens from 3M and reduced and analyzed data from 254 images. The tests compared the effect of altering cure schedules of anisotropic conductive adhesives contained in the chip-on-glass specimens. Initial tests were conducted at Intel's request to assess the feasibility of using e-beam moiré to provide data on interconnect structures, suitable for use in modeling. Recently Intel approached NIST seeking new tools to aid in answering reliability issues that are anticipated from the packaging group. One technique that they are investigating is e-beam moiré. A visit to Intel was made at which a presentation of the technique was made.

Two specific areas to be addressed in the next year are production of grids that can withstand thermal cycling, and finding methods for decreasing the pitch of the grids in order to improve resolution. Once the thermal cycling issue is resolved, the technique will be applied to measurements of thermal fatigue of advanced packaging structures. To create the smaller-pitch arrays that will be needed as chip and packaging technology advances, we plan to investigate the feasibility of performing lithography with our AFM. In addition, a comprehensive document describing the e-beam moiré method will be prepared to assist in technology transfer of this technique. We will be continuing our participation at the request of Intel (AZ) in an evaluation of nanoscale displacement measurement techniques and at the request of Intel (OR) in use of the e-beam moiré to measure displacements within on-chip layered interconnect structures.

From the 1997 NTRS, page 150: "Key is development of in situ model mechanics elucidation and validation tools such as micro-moiré, nano indentation techniques, and interface fracture toughness techniques." At present, project collaborations are underway with 3M, Intel (AZ), Intel (OR).

Contacts: Ms. Elizabeth Drexler, phone: (303) 497-5350, e-mail: drexler@boulder.nist.gov
Dr. David T. Read, phone: (303) 497-3853, e-mail: read@boulder.nist.gov

Hygrothermal Expansion of Polymer Thin Films

Polymers are widely used in electronic packaging in many applications. These include interlayer dielectrics, underfills in ball grid arrays, adhesives, encapsulants, and substrates. In many of these applications, the polymer is in the form of a thin film on another material with significantly different physical properties. Knowing and predicting the dimensional changes of these films with temperature and humidity are important for modeling the performance and reliability of complex assemblies. The properties of these films can be significantly different from the material in bulk form, especially in a constrained geometry. In addition, these materials may only be available in the form of thin films. The most commonly used technique, thermomechanical analysis (TMA), has been previously demonstrated by round robin tests to be inadequate for determining these very small changes in film thickness.

This effort has the primary objective of providing industry with robust measurement tools and data for characterizing the dimensional stability of polymers. In particular, the project is focused on the measurement of changes with temperature and humidity on the out-of-plane dimensions of thin films. NIST has designed, built, and demonstrated a capacitance cell with outstanding sensitivity for measuring the out-of-plane expansion of polymer films. The project has three sets of activities: (1) determining the accuracy and precision of the technique applied to a variety of polymer measurements; (2) working with standards-setting bodies to explore the desirability of introducing the technique as a standard method for measuring thermal and hygroscopic expansion; and (3) providing industry with materials property data on selected packaging materials.

In the first set of activities related to precision and accuracy, we are concluding extensive studies to determine the measurement uncertainty and limitations of the current capacitance-cell design and measurement method. This includes sample preparation and handling, determination of temperature differentials within the environmental chamber, and measurement of standard samples - single crystal (0001) orientation Al_2O_3. Additionally, the errors propagated from the uncertainties in the humidity and PVT properties of air and water are being evaluated. In the second set of activities, we plan to work with the test methods committees of IPC, SEMI, and ASTM to have the capacitance technique considered as an additional standard test method for the measurement of thermal expansion for cases in which the existing standards are inappropriate. Finally, in the course of the work, data on several materials of importance to the electronics industry have been and will be generated and disseminated through the appropriate venues. We expect to provide measurement expertise to appropriate audiences, such as the 1998 International Conference on Characterization and Metrology for ULSI Technology.

The 1997 NTRS states on page 113 "Areas of concern with the new materials and architectures are as follows: in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), line resistivity (versus bulk resistivity), available of high frequency dielectric constant values... " In addition polymer dielectrics and standards for materials and processing are mentioned on page 150 and in Table 51 on page 149. This project is working to introduce the measurement standards needed to describe thin films used in these applications.

Contacts: Dr. Frederick I. Mopsik, phone: (301) 975-6747, e-mail: fim@nist.gov
Dr. Chad R. Snyder, phone: (301) 975-4526, e-mail: chad.snyder@nist.gov

Solderability Measurements for Microelectronics

The decrease in dimensions of electronic devices has resulted in a dramatic increase in interconnection density. This development has introduced new stringent demands on solder and the soldering process and produced a need for improved solderability tests and standards. To meet this need, NIST is developing test techniques and scientific guidelines that U.S. manufacturers can use to evaluate solder and solderability of components before committing them to the production line. Both Pb-Sn and Pb-free solder alloys are being addressed.

Improved solderability test methods will lead to increased manufacturability and reliability in microelectronic devices. Such increased reliability and predictability for solder joints is essential for U.S. industry in producing fine pitch surface mount and ball grid array interconnects, where small size scales and limits on visual inspection of the solder joint make rework of improperly soldered connections difficult or impossible.

To aid in the interpretation and improvement of the frequently used wetting balance test for solderability, where a component is dipped into a solder bath and dynamic wetting occurs, effects of temperature and atmosphere on wettability and interactions between solders and substrates have been measured. Results from this work are being incorporated into the revision of ANSI/J-STD-002 (Joint Industry Standard on Solderability Tests for Component Leads, Terminations, Lugs, Terminals, and Wires) currently being finalized by the Institute for Interconnecting and Packaging Electronic Circuits (IPC).

The growth of oxides on surfaces is a frequent cause of loss of solderabilty of printed wiring boards and components during storage. Electrochemical tests, especially sequential electrochemical reduction analyses (SERA), are being applied to measure the chemical nature of the species produced by oxidation, the structures and thicknesses of the surface layers, their role in the degradation of solderability on copper substrates, and the effectiveness of imidazole oxidation inhibitors.

These solderability issues are driven by the smaller pitch and footprints of leads on BGA and surface mount devices and by concerns raised by the advent of lead-free solders which will inevitably involve changes in soldering techniques. Industry is pursuing significant pitch reduction goals, as described in the Assembly and Packaging Section of the 1997 NTRS, Table 46 on page 142, and in Tables 47 and 48 on page 143. The IPC National Technology Roadmap for Electronic Interconnections (1997) in its assembly materials section identifies improved solderability tests and lead-free solders as needs to achieve industry goals projected for the next 2 to 4 years.

Contacts: Dr. John R. Manning, phone: 301-975-6157, e-mail: manning@nist.gov
Dr. Frank W. Gayle, phone: 301-975-6161, e-mail: frank.gayle@nist.gov

DESIGN

Metrology for Simulation and Computer Aided Design

Compact Device Electrical Models. Only recently has there been a significant effort in developing an infrastructure for validating the performance of compact models. An example of this activity is the NIST/IEEE Model Validation Working Group, founded in 1994 and now having over 200 members from 100 different technical organizations. This group's activities are discussed on its Web page at http://ray.eeel.nist.gov/modval.html.

This working group has proposed two model validation standards projects that have been approved by the IEEE Standards Board: IEEE standard P1464 for Insulated Gate Bipolar Transistor (IGBT) Circuit Simulator Model Validation and IEEE standard P1485 for Micro-Electronic MOSFET Circuit Simulator Model Validation. The EIA Compact Model Council (formerly the SEMATECH Compact Model Council) has also joined the NIST/IEEE Working Group on Model Validation in the development of the Micro-Electronic MOSFET Model Validation Standard. The first draft of this standard was completed and posted on the Working Group web site, and a balloting committee is in the process of being formed.

In addition to founding and supporting the NIST/IEEE Working Group on Model Validation, the project has extensive laboratory efforts in this area. A test bed has been developed for validating the electrical performance of compact IGBT models. This test bed has been applied to evaluate the IGBT component libraries in commercial circuit simulators. As a result of this validation study, a major circuit simulator software vendor has made changes that substantially improve the accuracy of their IGBT component library. An additional test method based upon soft switching topologies is also being developed.

Compact Package Thermal Models. The accurate and timely simulation of the thermal performance of systems has become more important as competitive pressures have forced reduced development times. All of the complexities and details of the thermal aspects of electronic systems cannot be efficiently included in a system level simulation, though. Simplified or "compact" thermal models must be used for the components, such as micro-electronic packages and circuit boards. The objective of this task is to develop methodologies to validate the performance and accuracy of compact package thermal models for use in system level thermal simulations for all types of applications.

The first application selected was for horizontally mounted packages in a natural convection environment. A test bed was selected based upon an EIA/JEDEC-recommended free, natural convection test enclosure. Simulations were performed for a detailed package model and several compact package models. It was found that, while system level considerations, especially circuit board conductivity and radiative heat transfer, had to be well characterized, the enclosure could be used to validate compact model performance. The experiments included temperature measurements with thermocouples and thermal test chips and flow visualization by smoke injection. The models validated in the free convection enclosure have been used to simulate the thermal behavior of a 3 by 3 array of packages in a confined, narrow aspect enclosure, representative of a lap top computer. This is the first-ever demonstration of a procedure using a realistic but simplified standard test bed to validate the performance of package thermal models for use in real systems applications. This work is described in several archival publications and several conference papers.

Package Electrical Interconnect Models. An effort has recently been undertaken to develop systematic methods for including the effects of package interconnect parasitics into circuit and system simulation. Interconnect structures are becoming a dominant factor in limiting the performance of modem computer, communication, and power systems. The Time Domain Reflectometry (TDR) technique is being examined to characterize various semiconductor interconnect systems, multi chip modules, and discrete packages. Appropriate test fixtures are being developed to launch the TDR signal in a configuration that represents the application condition for the interconnect being measured, and methods are being developed to reduce the complexity of the interconnect models by accounting for the range of application conditions that a particular interconnect model must simulate accurately. Also, finite element interconnect simulation tools are being used to validate the compact interconnect models developed using the experimental TDR method.

Metrology and modeling of packages are both discussed on page 132 of the 1997 NTRS. NIST has long been a strong contributor on these topics. The wide divergence between power levels for hand-held vs. high-performance applications as discussed in Table 37 on page 115 underscores the need for improved package designs as described on page 136. These can only be obtained with the aid of improved 3D models and the necessary data on materials properties to support them.

Contact: Dr. Allen R. Hefner, phone: (301) 975-2071, e-mail: allen.hefner@nist.gov

APPENDICES

Appendix A: Abbreviations and Acronyms

AFM, atomic force microscope
ALMWG, Analytical Lab Managers Working Group
ASME, American Society for Mechanical Engineers
ASTM, American Society for Testing and Materials
BRDF, bidirectional reflectance distribution function
C-AFM, calibrated metrology AFM
C-V, Capacitance-Voltage
CCD, charged coupled device
CD, critical dimension
CFM, contamination-free manufacturing
CMOS, complementary metal-oxide semiconductor
CMP, chemo-mechanical polishing
CRADA, Cooperative Research and Development Agreement
CRDS, cavity ring-down spectroscopy
CVD, chemical vapor deposition
DIN, Deutsches Institut für Normung
DUV, deep ultraviolet
EELS, Electron Energy Loss Spectrometry
EIA, Electronics Industry Association
GEC, Gaseous Electronics Conference
GIXPS, grazing incidence X-ray photoelectron spectroscopy
GOSI, goniometric optical scatter instrument
IEEE, Institute of Electrical and Electronics Engineers
IGBT, insulated gate bipolor transistor
IPC, Institute for Interconnecting and Packaging Electronic Circuits
ISO, International Organization for Standardization
JEDEC, Joint Electron Device Engineering Council
LFPG, low frost-point humidity generator
MIT, Massachusetts Institute of Technology
NIST, National Institute of Standards and Technology
NSMP, National Semiconductor Metrology Program
NTRM, NIST Traceable Reference Material
PEVCD, plasma enhanced chemical vapor deposition
PPM, scanning proximal probe
RGAs, residual gas analyzers
RM, reference material
RTP, rapid thermal processing
SBIR, Small Business Innovation Research program
SCM, scanning capacitance microscope
SEM, scanning electron microscope
SEMATECH, SEiconductor MAufacturing TECHnology
SEMI/SEMATECH, Semiconductor Equipment and Materials International/SEmiconductor MAnufacturing TECHnology
SEMI, Semiconductor Equipment and Materials International
Si, silicon
SIMS, secondary ion mass spectrometry
SiO_2, Silicon dioxide
SOI, silicon-on-insulator
SOSI, scanning opitcal scatter instrument
SPM, scanning probe instruments
SRM, Standard Reference Material
TCAD, technology computer aided design
TEM, transmission electron microscopy
TDDB, time-dependent dielectric breakdown
TDR, time domain reflectometry
TMA, thermomechanical analysis
UV, ultraviolet

Appendix B: Key Words Index

1D, 6
2D, 6, 22
2D measurements, 6
2D profiling, 22
3D, 22
3D profiling, 22
100 nm, 8
150 nm, 19
157 nm, 7
193 nm, 7, 8
193 nm excimer laser engery and dose meters, 8
248 nm, 7, 8
300 nm, 19
1998 International Conference on Characterization and Metrology for ULSI Technology, 27
AFM, 2, 26
Analytical Lab Managers Working Group (ALMWG), 17
ASTM, 23, 27
atomic force microscope (AFM), 2, 26
bibliography, 11
bidirectional ellipsometry, 16
bidirectional reflectance distribution function (BRDF), 16
bow, 19
BRDF, 16
C-AFM, 2
C-V, 21
calcium fluoride, 7
calibrated metrology AFM (C-AFM), 2
calibration, 8, 9, 14
calibration facility, 8
calibration procedures, 9
calibration wafers, 14
capacitance-voltage (C-V), 21
Cavity Ring-Down Spectroscopy (CRDS), 10
CCD, 5
CD, 4, 5
CD and overlay calibration, 4
chamber cleaning, 11
charged coupled device (CCD), 5
chemical analysis, 17
chemical characterizations, 18
chemo-mechanical polishing (CMP), 19
chemical-mechanical polishing (CMP), 24
chuck flatness/thickness, 19
CMOS, iii, 18
CMP, 19, 24
compact device electrical models, 29
compact package thermal models, 29
conductors, 24
confocal microscope, 5
contaminant gases, 9
contamination-free manufacturing, 12
control equipment, 9
coplanar waveguide, 25
copper films, 24
CRADA, 1, 2, 14
CRDS, 10
current-voltage (I-V)
CVD, 11, 12
CVD process measurements, 11
CVD reactor, 12
Deep Ultraviolet (DUV), 7, 8
Deep Ultraviolet (DUV) Laser Metrology, 8
Deep Ultraviolet (DUV) Lithography, 7
defects, 16
depth profiling, 22
depth profiling reference materials, 22
design, 29
detector calibrations, 7
device failure, 18
dielectric, 20, 23, 25
dielectric films, 20
dielectric integrity, 23
differential mobility analyzer (DMA), 15
dimensional metrology, 1, 2, 3, 4
diode-laser-based-hygrometer, 10
dopant concentration, 21
dopant profiling goals, 21
dose, 7, 8
DUV, 7, 8
DUV laser metrology, 8
DUV lasers, 8
e-beam moiré, 26
EELS, 18
EIA, 29
electrical CD, 4
electrical linewidth, 4
electromagnetic characterization, 25
electromagnetic properties of thin-films, 25
electromigration studies, 24
electron-beam, 18, 26
electron-beam moiré, 26
Electron Energy Loss Spectrometry (EELS), 18
electronic packaging, 26, 27
ellipsometry, 20
Emulated Stepper Aerial Image Measurement, 5
energy and dose transfer standards, 8
etching and deposition plasmas, 11
fab processes, 11
FASTC2D SCM, 21

flat-panel display, 6
flatness, 19
flowmetering, 9
front-end processes, 19, 20, 21, 22, 23
gas, 9, 10, 11, 12
gas phase, 12
gas phase concentrations, 10
gas pressure, 9
Gaseous Electronics Conference (GEC), 11
gases, 9
gate dielectrics, 20
gate electric fields, 23
gate films, 20
gate oxides, 23
GEC rf Reference Cell, 11
GIXPS, 18
Goniometric Optical Scatter Instrument (GOSI), 16
GOSI, 16
grazing incidence X-ray photoelectron spectroscopy (GIXPS), 18
high-resolution field emission SEM, 1
humidity, 10, 27
hygrometer, 10
hygrothermal, 27
hygrothermal expansion of polymer thin film, 27
I-V, 20
IGBT, 29
image-depth-profiling method, 22
IMGC, 13
index issues, 7
index measurements, 7
Institute for Interconnecting and Packaging Electronic Circuits (IPC), 28
insulated gate bipolar transistor (IGBT), 29
interconnect, 24, 26, 29
interconnect films, 24
interconnect materials, 24
interconnection density, 28
interferometer, 6, 19
interlayer dielectrics, 27
interlevel dielectrics, 25
IPC, 27, 28
JEDEC, 23, 29
laminar flowmeter transfer standards, 9
lead-free solder (Pb-free solder), 28
LFPG, 10
light scatter, 16
linescale interferometer, 6
linewidth, 3, 4, 5
linewidth correlation, 3
linewidth reference materials, 4
linewidth standards, 3, 5
lithography, 1, 2, 3, 4, 5, 6, 7, 8
low dielectric-constant materials, 25
low frost-point humidity generator (LFPG), 10
mass flow, 9
mechanical properties of thin films, 24
metal multilayers, 22
micro structural processes, 24
microanalysis, 17
microcalorimeter, 17
microcontamination, 12
microstrip, 25
MIT Lincoln Laboratory, 7, 8, 18
model validation, 29
modeling, 12
models, 21
MOSFET, 29
nanometer level, 1
neutron scattering, 20
NIST Traceable Reference Material (NTRM), 20
NTRM, 20
optical CD, 5
optical function data, 20
optical materials metrology, 7
optical scattering, 16
overlay metrology, 4, 5
oxide thickness, 23
p-n junctions, 21
package models, 29
packaging, 26, 27, 28
packaging materials, 27
packaging structures, 26
particle, 12, 15, 16, 18
particle analysis, 18
particle composition, 18
particle contaminants, 18
particle contamination on wafers, 15
particle formation, 12
particle growth, 12
particle measurements, 15
particle size, 15
particle transport, 12
Pb-free solder (lead-free solder), 28
PC board, 6
photolithography, 7
photomask linewidths, 5
physics of failure, 23
plasma, 11
plasma process, 11
plasma uniformity, 11
polishing, 19
polymer, 27
PPM, 1
process monitoring, 9
processing, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18
radiometer in-situ calibration, 14
radiation thermometers, 14

radiometers, 14
radiometric, 7
rapid thermal processing (RTP), 14
reliability, 23, 24
reliability metrology, 24
reliability testing, 23
residual gas analyzers (RGAs), 9, 20
reticles, 6
RGAs, 9, 20
RM 8090, 1
rotating disk, 12
RTP, 14
RTP Advisory Group Meeting, 14
SBIR, 6
scanning capacitance microscope (SCM), 21 scanning
electron microscope (SEM), 1
Scanning Optical Scatter Instrument (SOSI), 16
scanning probe microscopy, 21
scanning proximal probe (PPM), 1
scanning surface inspection system, 16
secondary ion mass spectrometry (SIMS), 22
SEM, 1
SEMI, 27
SEMATECH, 5, 7, 8, 17, 22, 24, 25
SEMI/SEMATECH, 9
SEMI/SEMATECH Thermal Mass Flow Meter
Working Group, 9
sequential electrochemical reduction analyses
(SERA), 28
SERA, 28
silica, 7
Silicon-on-Insulator (SOI) CMOS, 18
silicon wafers, 16, 19
SOI CMOS, 18
solderability measurements, 28
solderability test methods, 28
SOSI, 16
source standards, 7
SRM, 1, 3, 5, 15, 22
SRM 2091, 1
SRM 2134, 22
SRM 2800, 5
Standard Reference Material (SRM), 1, 3, 5, 15, 22
standards, 9
stress voiding, 24
stress voiding and electromigration, 24
technology computer-aided design (TCAD), 21
telepresence microscopy and microanalysis system, 18
TEM, 2, 18
temperature, 13, 14, 27
temperature measurement, 14
TES, 17
TES microcalorimeter, 17
test chip design, 4
thermal fatigue, 26
thermal, 9, 26, 27
Thermal Mass Flow Meter Working Group, 9
thermal cycling, 26
thermocouples, 13
thermomechanical analysis (TMA), 27
thermometry, 13
thickness variation, 19
thin films, 18, 24, 25, 27
thin dielectric films, 20
thin-film, 24
thin-film conductors, 24
thin-film characterization, 25
thin-film thermocouples, 14
three-dimensional dopant profiles, 21
time domain reflectometry (TDR), 29
time-dependent dielectric breakdown (TDDB), 23
transition-edge sensor (TES), 17
Transmission Electron Microscopy (TEM), 18
transmission-line measurement, 25
ultra-high depth resolution, 22
ultra-high depth resolution profiling, 22
ultra-shallow profiling, 22
ultra-thin dielectric reliability metrology, 23
ultra-thin gate oxides, 23
Ultraviolet (UV), 7, 8, 16
UV, 7, 8, 16
vacuum chucks, 19
wafer, 14, 19
wafer radiation environment, 14
wafer and chuck flatness/thickness, 19
water vapor, 10
wetting balance test for solderability, 28
X-ray, 17, 18, 20
X-ray detector, 17
X-ray emission analysis, 18
X-ray spectrometry, 18

Appendix C: Recent Publications

Listed below are NSMP project-related publications from calendar year 1997. These NSMP project-related publications, as well as those dating back through 1990, are also included within the *NIST List of Publications 103, National Semiconductor Metrology Program and the Semiconductor Electronics Division, LP 103,* March 1998.

1. Adams, V. H., Blackburn, D. L., Joshi, Y., and Berning, D. W., Issues in Validating Package Compact Thermal Models for Natural Convection Cooled Electronic Systems, *IEEE Trans. Components, Packaging, and Manufacturing Technology*, Part A, 20 (4), 420-431 (December 1997). [Also published in the Proceedings of the Thirteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium - SEMITHERM XIII, January 28-30, 1997, Austin, Texas, pp. 10-23.]

2. Adams, V. H., Joshi, Y., and Blackburn, D. L., Application of Compact Model Methodologies to Natural Convection Cooling of an Array of Electronic Packages in a Low Profile Enclosure, *Advances in Electronic Packaging 1997*, Proceedings of the Pacific Rim/ASME International Intersociety Electronic and Photonic Packaging Conference, INTERpack '97, Kohala Coast, Hawaii, June 15-19, 1997, pp. 1967-1974.

3. Adams, V. H., Joshi, Y., and Blackburn, D.L., Package Geometry Considerations in Thermal Compact Modeling Strategies, Proceedings of the Conference on Thermal Management of Electronic Systems, EUROTHERM 58, Nantes, France, September 24-26, 1997, pp. 136-144.

4. Belzer, B. J., and Blackburn, D. L., *Semiconductor Measurement Technology*: The Results of an Interlaboratory Study of Ellipsometric Measurements of Thin Film Silicon Dioxide on Silicon, NIST Special Publication 400-99 (May 1997).

5. Berger, J. R., and Tewary, V. K., Boundary Element Analysis of Moiré Fields in Anisotropic Materials, *Engineering Analysis with Boundary Elements* **18** (4), 317-325 (1996).

6. Burns, T. J., Davis, R. W., and Moore, E. F., Dynamical Systems Approach to Particle Transport Modeling in Dilute Gas-Particle Flows with Application to a Chemical Vapor Deposition Reactor, *Aerosol Sci. & Tech.* **27** (1), 1-21 (1997).

7. Chen, W.T., Questad, D., Read, D., and Sammakia, B., Opportunities and Needs for Interfacial Fracture Mechanics in Microelectronic Packaging Industry, in *Application of Fracture Mechanics in Electronic Packaging*, Proceedings of ASME IMECE 1997, Dallas, Texas, November 18, 1997, D. T. Read and W. T. Chen, Ed., pp. 183-192.

8. Chi, P. H., Simons, D. S., Wickenden, A. E., and Koleske, D. D., Repeatability of Si Concentration Measurements in Si-Doped GaN Films, *J. Vac. Sci. Technol. A* **15**, 2565-2568 (1997).

9. Christophorou, L. G., Olthoff, J. K., and Rao, M. V. V. S., Electron Interactions with CHF_3, *J. Phys. Chem. Ref. Data* **26**, 1205-1237 (1997).

10. Christophorou, L. G., Olthoff, J. K., and Wang, Y., Electron Interactions with CCl_2F_2, Proceedings of the 23d International Conference on Phenomena in Ionized Gases, Toulouse, France, July 17-22, 1997, pp. I-68--I-69.

11. Christophorou, L. G., Olthoff, J. K., and Wang, Y., Electron Interactions with CCl_2F_2, *J. Phys. Chem. Ref. Data* **26**, 1205 (1997).

12. Clement, J. J., Keller, R. R., Krisch, K. S., Sanchez, J. E., Jr., and Suo, Z., Eds., *Materials Reliability in Microelectronics VII*, Vol. 473 (Materials Research Society, 1997), 457 pages.

13. Cresswell, M. W., Allen, R. A., Linholm, L. W., Guthrie, W. F., Penzes, W. B., and Gurnell, A. W., Hybrid Optical-Electrical Overlay Test Structure, *IEEE Trans. Semicond. Mfg.* **10** (2), 250-255 (May 1997).

14. Cresswell, M. W., Sniegowski, J. J., Ghoshtagore, R. N., Allen, R. A., Guthrie, W. F., and Linholm, L. W., Electrical Linewidth Test Structures Fabricated in Mono-Crystalline Films for Reference-Material Applications, Proceedings of the 1997 IEEE International Conference on Microelectronic Test Structures, Monterey, California, March 17-20, 1997, pp. 16-24.

15. Dickens, B., Photoacoustic Infrared Spectroscopy of Thin Polyimide Layers on Glass Substrates, NISTIR 6097 (1997).

16. Dixson, R., Tsai, V. W., Vorburger, T. V., Williams, E. D., Wang, X. S., Fu, J., and Koning, R., Measurements of Pitch, Height, and Width Artifacts with the NIST Calibrated Atomic Force Microscope, Proceedings of the 1997 ASPE Spring Topical Meeting on Advances in Surface Metrology, Vol. 15, Annapolis, Maryland, June 2 -5 1997, pp. 70-75.

17. Djurovic, S., Roberts, J. R., and Olthoff, J. K., Spatial and Time Characteristics of Low Temperature rf Plasmas for Materials Processing, *J. Magnetohydrodynamics and Plasma Res.* **7**, 1-18 (1997).

18. Dufaux, D. P., and Zachariah, M. R., Aerosol Mineralization of Chlorofluorocarbons by Sodium Vapor Reduction, *Environmental Science and Technology* **31** (8), 223-228 (1997).

19. Ehrstein, J. R., and Croarkin, M. C., *Standard Reference Materials*: The Certification of 100 mm Diameter Silicon Resistivity SRMs 2541 through 2547 Using Dual-Configuration Four-Point Probe Measurements, NIST Special Publication 260-131 (August 1997).

20. Germer, T. A., Angular Dependence and Polarization of Out-of-Plane Optical Scattering from Particulate Contamination, Subsurface Defects, and Surface Microroughness, *Appl. Opt.* **36**, 8798-8805 (1997).

21. Germer, T. A., and Asmail, C. C., Bidirectional Ellipsometry and Its Application to the Characterization of Surfaces, Proceedings of the SPIE, The International Society for Optical Engineering, *Polarization: Measurement, Analysis, and Remote Sensing* **3121**, 173-182 (1997).

22. Germer, T. A., and Asmail, C. C., A Goniometric Optical Scatter Instrument for Bidirectional Reflectance Distribution Function Measurements with Out-of-Plane and Polarimetry Capabilities, Proceedings of the SPIE, The International Society for Optical Engineering, *Scattering and Surface Roughness* **3141**, 220-231 (1997).

23. Germer, T. A., Asmail, C. C., and Scheer, B. W., Polarization of Out-of-Plane Scattering from Microrough Silicon, *Opt. Lett.* **22**, 1284-1286 (1997).

24. Gillen, G., Bright, D., Lorincik, J., and Mogren, S., Quantitative 3D Image Depth Profiling SIMS: Characterization of Patterned Ion Implants in Silicon, in *Secondary Ion Mass Spectrometry SIMS X*, A. Benninghoven et al., Eds. (Chichester, John Wiley and Sons, 1997), pp. 321-324.

25. Janezic, M. D., and Williams, D. F., Permittivity Characterization from Transmission-Line Measurement, IEEE International Microwave Symposium Digest, Denver, Colorado, June 10-13, 1997, paper TH2D-5 .

26. Keller, R. R., and Nucci, J. A., Effects of Local Crystallography on Stress-Induced Voiding in Passivated Copper Interconnects, NATO Advanced Study Institute Series: Electron Crystallography, Sicily, Italy, May 22-June 2, 1997.

27. Keller, R. R., Nucci, J. A., and Field, D. P., Local Textures and Grain Boundary Structure Characterization in Voided Copper Interconnects, *J. Electron. Mat.* **26**, 996-1001 (1997).

28. Koning, R., Dixson, R., Fu, J., Tsai, V. W., Vorburger, T. V., Williams, E. D., and Wang, X. S., Pitch and Step Height Measurements Using the Calibrated Atomic Force Microscope, Proceedings of the 1997 Conference on Quantitative Microscopy, Vienna, Austria, November 5-7, 1997, PTB report F-30, K. Hasche, W. Mirande, and G. Wilkening, Eds. (PTB, Braunschweig, Germany, 1997), pp. 172-176.

29. Kopanski, J. J., Marchiando, J. F., and Alvis, R., Practical Metrology Aspects of Scanning Capacitance Microscopy for Silicon 2-D Dopant Profiling, in *Diagnostic Techniques for Semiconductor Materials and Devices,* Proceedings of the Conference, Vol. 97-12, P. Rai-Choudhury, J. L. Benton, D.K. Schroder, and T. J. Shaffner, Eds. (The Electrochemical Society, Inc., Pennington, New Jersey), pp. 183-193.

30. Kopanski, J. J., Marchiando, J. F., Berning, D. W., Alvis, R., and Smith, H. E., Scanning Capacitance Microscopy Measurement of 2-D Dopant Profiles across Junctions, Proceedings of the Fourth International Workshop on Measurement, Characterization and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, Research Triangle Park, North Carolina, April 6-9, 1997, pp. 53.1-53.9.

31. Kopanski, J. J., Marchiando, J. F., and Lowney, J. R., Scanning Capacitance Microscopy Applied to Two-Dimensional Dopant Profiling of Semiconductors, *Materials Science & Engineering B* **44**, 46-51 (1997).

32. Lee, W. F., Guthrie, W. F., Cresswell, M. W., Allen, R. A., Sniegowski, J. J., and Linholm, L. W., Reference-Length Shortening by Kelvin Voltage Taps in Linewidth Test Structures Replicated in Mono-Crystalline Silicon Films, Proceedings of the 1997 IEEE International Conference on Microelectronic Test Structures, Monterey, California, March 18-20, 1997, pp. 35-38.

33. Liggett, W., Moon, K.-W., and Handwerker, C., An Experimental Method for Refinement of Solderability Measurement, *Solderability and Surface Mount Technology* **26**, 14-21 (July 1997).

34. Lorincik, J., Fine, J, and Gillen, G., The Scanning Scattering Microscope for Surface and Buried Interface Roughness and Defect Imaging, Proceedings of the SPIE, The International Society for Optical Engineering, *Scattering and Surface Roughness* **3141**, 302-315 (1997).

35. Mantooth, H. A., and Hefner, A. R., Jr., Electrothermal Simulation of an IGBT PVM Inverter, *IEEE Trans. Power Electronics* **12** (3), 474-484 (1997). [Same as 93-48]

36. Marchiando, J. F., Kopanski, J. J., and Lowney, J. R., A Model Database for Determining Dopant Profiles from Scanning Capacitance Microscope Measurements, Proceedings of the Fourth International Workshop on Measurement, Characterization and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, Research Triangle Park, North Carolina, April 6-9, 1997, pp. 65.1–65.3.

37. Martin, A., O'Sullivan, P., Mathewson, A., Suehle, J. S., and Chaparala, P., Investigation of the Influence of Ramped Voltage Stress on Intrinsic t_{bd} of MOS Gate Oxides, *Solid State Electron.* **41** (7), 1013-1020 (1997).

38. Martinis, J. M., Wollman, D. A., Irwin, K. D., and Hilton. G. C., Microcalorimeter X-Ray Spectrometers, *Future Fab International* **1** (3), 333 (1997).

39. McMillin, B. K., and Zachariah, M. R., Two-Dimensional Imaging of CF_2 Density by Laser-Induced Fluorescence in CF_4 Etching Plasmas in the Gaseous Electronics Conference Reference Cell, *J. Vac. Sci. Technol. A* **15** (2), 230-237 (1997).

40. Nguyen, N. V., and Richter, C. A., Thickness Determination of Ultra-Thin SiO_2 Films on Si by Spectroscopic Ellipsometry, in *Silicon Nitride and Silicon Dioxide Thin Insulating Films*, Proceedings of the Conference, Vol. 97-10, M. J. Deen, W. D. Brown, K. B. Sundaram, and S. I. Raider, Eds. (The Electrochemical Society, Inc., Pennington, New Jersey), pp. 183-193

41. Nucci, J. A., Keller, R. R., Field, D. P., and Shacham-Diamand, Y., Grain Boundary Misorientation Angles and Stress-Induced Voiding in Oxide Passivated Copper Interconnects, *Appl. Phys. Lett.* **70**, 1242-1244 (1997).

42. Olthoff, J. K., Plasma Diagnostics on the Gaseous Electronics Conference Radio-Frequency Reference Cell, Proceedings of the Conference on Frontiers in Low Temperature Plasma Diagnostics II, Bad Honnef, Germany, February 17-21, 1997, pp. 47-56.

43. Park, B. C., Vorburger, T. V., Germer, T. A., and Marx, E., Scattering from Sinusoidal Gratings, Proceedings of the SPIE, The International Society for Optical Engineering, *Scattering and Surface Roughness* **3141**, 65-77 (1997).

44. Postek, M. T., The Development of an Industrial Standard (Standard Reference Material) SRM 2090. Management Project to the University of Maryland, University College Graduate School of Management and Technology, Executive Masters of Science in Technology Management (1997), 136 pages.

45. Postek, M. T. , The Potentials for Inspection and Metrology of MEMS Using a Combined Scanning Electron Microscope (SEM) and Proximal Probe Microscope (PPM), Proceedings of the SPIE, The International Society for Optical Engineering, *Microlithography and Metrology in Micromachining III* **3225**, 92-101 (1997).

46. Postek, M. T., The Scanning Electron Microscope, in *Handbook of Charged Particle Optics*, Jon Orlof, Ed. (CRC Press, Inc., New York), pp. 363-399.

47. Postek, M. T., and Ho, H., Dimensional Metrology at the Nanometer Level: Combined SEM and AFM, Proceedings of the SPIE, The International Society for Optical Engineering, *Metrology, Inspection, and Process Control for Microlithography XI* **3050**, 250-263 (1997).

48. Postek, M. T., and Vladar, A. E., Inexpensive Digital Imaging? *Scanning* **19**, 297-299 (1997).

49. Postek, M. T., Vladar, A. V., and Davidson, M., Fourier Transform Feedback Tool for Scanning Electron Microscopes Used in Semiconductor Metrology, Proceedings of the SPIE, The International Society for Optical Engineering, *Metrology, Inspection, and Process Control for Microlithography XI* **3050**, 68-79 (1997).

50. Postek, M. T., Vladar, A. E., and Davidson, M. P., Performance Analysis Tool for Scanning Electron Microscopes Used in Semiconductor Metrology, *Scanning* **19** (3), 223-234 (1997).

51. Potzick, J., *Standard Reference Materials:* Antireflecting-Chromium Linewidth Standard, SRM 473, for Calibration of Optical Microscope Linewidth Measuring Systems, NIST Special Publication 260-129 (1997).

52. Potzick, J., New NIST-Certified Small Scale Pitch Standard, Proceedings of the 1997 Measurement Science Conference, Pasadena, California, January 1997. [(Also appeared in *Cal Lab Magazine* **4** (3), 18-24 (May/June 1997).]

53. Potzick, J., Photomask Metrology in the Era of Neolithography, Proceedings of the 17th Annual BACUS/SPIE Symposium, *Photomask Technology and Management*, **3236**, 32 (Sept. 1997).

54. Rao, M. V. V. S., Olthoff, J. K., Christophorou, L. G., and Van Brunt, R. J., Negative Ion Kinetic-Energy Distributions and Ion-Neutral Reactions in O_2 and CO_2 Townsend Discharges at High E/N, Proceedings of the International Symposium on Electron-Molecule Collisions and Ion and Electron Swarms, Engelberg, Switzerland, July 19-22, 1997, pp. 60/1-60/2.

55. Rao, M. V. V. S., Olthoff, J. K., and Van Brunt, R. J., Translational Kinetic-Energy Distributions of Positive Ions Produced in Townsend Discharges of SF_6 at High Electric Field-to-Gas Density Ratios (E/N), Proceedings of the 20th International Conference on the Physics of Electronic and Atomic Collisions, Vienna, Austria, July 23-29, 1997, Abstract no. MO203.

56. Rao, M. V. V. S., Olthoff, J. K., and Van Brunt, R. J., Negative Ion Energy Distributions and Ion-Neutral Reactions in SF_6 Townsend Discharges at High Electric Field-to-Gas Density Ratios (E/N), Proceedings of the 20th International Conference on the Physics of Electronic and Atomic Collisions, Vienna, Austria, July 23-29, 1997, p. MO202.

57. Rao, M. V. V. S., Van Brunt, R. J., and Olthoff, J. K., Kinetic-Energy Distributions of Positive Ions Produced in Townsend Discharges of Oxygen at High Electric Field-to-Gas Density Ratios, Proceedings of the International Symposium on Electron-Molecule Collisions and Ion and Electron Swarms, Engelberg, Switzerland, July 19-22, 1997, pp. 61/1-61/2.

58. Read, D. T., Piezo-Actuated Microtensile Test Apparatus, *Materials Technology* **12** (1), 12-14 (1997)

59. Read, D. T., and Chen, W. T., Eds., *Application of Fracture Mechanics in Electronic Packaging* (ASME IMECE, 1997), 193 pages.

60. Ripple, D., Burns, G., and Battuello, M., Highly Accurate Temperature Measurements with Pure Element Thermocouples, Proceedings of the 1997 National Conference of Standards Laboratories (NCSL) Workshop and Symposium, Atlanta, Georgia, July 27-31, 1997, pp. 481-488.

61. Roberts, J. R., Benck, E. C., and Schwabedissen, A., Overview of NIST GEC RF Reference Cell and ICP Projects, Proceedings of the 3rd International Conference on Reactive Plasmas and 14th Symposium on Plasma Processing, Nara, Japan, January 21-24, 1997, p. 61.

62. Robertson, L. S., Lilak, A., Law, M. E., Jones, K. S., Kringhoj, P. S., Rubin, L. M., Jackson, J., Simons, D. S., and Chi, P. The Effect of Dose Rate on Interstitial Release from the End-of-Range Implant Damage Region in Silicon, *Appl Phys. Lett.* **71**, 3105-3107 (1997).

63. Sanogo, O., and Zachariah, M. R., Kinetic Studies of the Reaction of Tetraethoxysilane with Oxygen Atoms, *J. Electrochem. Soc.* **144** (8), 2919-2923 (1997).

64. Schafft, H. A., Erhart, D. L., and Gladden, W. K., Toward a Building-In Reliability Approach, *Microelectron. Rel.* **37** (1), 3-18 (1997).

65. Schen, M. A., Wu, W., Wallace, W. E., Beck Tan, N., VanderHart, D., and Davis, G. T., Molecular Insights on Interfacial Properties and Moisture Uptake of Plastic Packaging Materials, Proceedings of the 3rd International Symposium and Exhibition on Advanced Packaging Materials, p. 85 (1997).

66. Schwabedissen, A., Benck, E. C., and Roberts, J. R., Influence of Different Coil Geometries on the Spatial Distribution of the Plasma Density in Planar Inductively Coupled Plasmas, *Phys. Rev. E* **56**, 5866-5875 (1997).

67. Schwabedissen, A., Benck, E. C., and Roberts, J. R., Langmuir Probe Measurements in an Inductively

Coupled Plasma Source, *Phys. Rev. E* **55**, 3450-3459 (1997).

68. Silver, R., Potzick, J., Scire, F., Evans, C., McLaughlin, M., Kornegay, E., and Larrabee, R., A Method to Characterize Overlay Tool Misalignments and Distortions, Proceedings of the SPIE, The International Society for Optical Engineering, *Metrology, Inspection, and Process Control for Microlithography XI* **3050**, 143-155 (1997).

69. Simons, D. S., The Depth Measurement of Craters Produced by Secondary Ion Mass Spectrometry - Results of a Stylus Profilometry Round-Robin Study, in *Secondary Ion Mass Spectrometry SIMS X*, A. Benninghoven et al., Eds. (Chichester, John Wiley and Sons, 1997), pp.435-438.

70. Sobolewski, M. A., Dynamic Model of the Radio-Frequency Plasma Sheath in a Highly Asymmetric Discharge Cell, *Phys. Rev. E* **56**, 1001-1010 (1997).

71. Sobolewski, M. A., Experimental Test of Models of Radio-Frequency Plasma Sheaths, *Appl. Phys. Lett.* **70**, 1049-1051 (1997).

72. Suehle, J. S., and Chaparala, P., Low Electric Field Breakdown of Thin SiO_2 Films under Static and Dynamic Stress, *IEEE Trans. Electron Dev.* **44** (5), 801-808 (May 1997).

73. Tea, N. H., Milanović, V., Zincke, C. A., Suehle, J. S., Gaitan, M., Zaghloul, M. E., and Geist, J., Hybrid Postprocessing Etching for CMOS-Compatible MEMS, *J. Microelectromechanical Systems* **6** (4), 363-372 (December 1997).

74. Thompson, P. E., Silvestre, C., Jernigan, G., Hobart, K., Simons, D. S., and Gregg, M., Effect of Ge on the Segregation of B in Si(100) and Si(110), *J. Appl. Phys.* **81**, 7317-7319 (1997).

75. Tilford, C. R., Optimizing Residual Gas Analyzers for Process Monitoring, Proceedings of the Symposium on Process Control, Diagnostics, and Modeling in Semiconductor Manufacturing, Vol. PV 97-7, M. Meyyappan, D. J. Economou, and S. W. Butler, Eds. (The Electrochemical Society, 1997), pp. 184-191.

76. Tison, S. A., and Berndt, L., High-Differential-Pressure Laminar Flowmeter, Proceedings of the 1997 ASME Fluids Engineering Summer Meeting, Vancouver, British Columbia, June 22-26, 1997, FEDSM97-3207 (1997).

77. Tison, S. A., and Doty, S.W., Low-Gas-Flow Proficiency Testing, Proceedings of the 1997 National Conference of Standards Laboratories (NCSL) Annual Meeting, Atlanta, Georgia, July 27-31, 1997, pp. 55-65.

78. Tsai, V. W., Wang, X. S., Williams, E. D., Schneir, J., and Dixson, R., Conformal Oxides on Si Surfaces, *Appl. Phys. Lett.* **71** (11), 1495-1497 (1997).

79. VanderHart, D. L., Davis, G. T., and Schen, M. A., NMR Determined Partitioning of Water Between Voids and the Polymer Matrix in an Electronics Packaging Material, APS Bulletin **42**, 464-465 (1997).

80. Villarrubia, J. S., Algorithms for Scanned Probe Microscope Image Simulation, Surface Reconstruction, and Tip Estimation, *J. Res. Natl. Inst. Stand. Technol.* **102**, 425-454 (1997).

81. Villarrubia, J. S., Blind Estimation of Tip Geometry in Scanned Probe Microscopy, Proceedings of Microscopy and Microanalysis '97, Cleveland, Ohio, August 10-14, 1997, Vol. 3, Supplement 2, pp. 1259-1260.

82. Vorburger, T. V., Evans, C. J., Tsai, V., Fu, J., Williams, E. D., Dixson, R., Sullivan, P. J., and McWaid, T., Finish and Figure Metrology for Soft X-Ray Optics, Proceedings of the Second U.S.-Japan Workshop on Soft X-Ray Optics: Technical Challenges, T. Namioka, H. Kinoshita, and K. Ito, Eds. (Japan Society for Precision Engineering, Tokyo, 1997), pp. 298-305.

83. Vorburger, T. V., Dagata J. A., Wilkening, G., and Iizuka, K., Industrial Uses of STM and AFM, *Annals of the CIRP* **47** (2) (1997).

84. Warren, J. A., Boettinger, W. J., and Roosen, A. R., Modeling Reactive Wetting, in *The Design and Reliability of Solders and Solder Interconnection*, R. K. Mahidhara, D. R. Frear, S. M. L. Sastry, K. L. Murty, P. K. Liaw, and W. L. Winterbottom, Eds. (TMS, Warrendale, Pennsylvania, 1997), pp. 155-157.

85. Williams, D. F., Calibration in Multiconductor Transmission Lines, 48th ARFTG Conference Digest, Orlando, Florida, Dec. 4-6, 1996, pp. 46-53.

86. Williams, D. F., Characterization of Embedded Multiconductor Transmission Lines, IEEE International Microwave Symposium Digest, Denver, Colorado, June 10-12, 1997, paper TH4D-2, pp. 1773-1776.

87. Williams, D. F., Multiconductor Transmission Line Characterization, *IEEE Trans. Components, Packaging, and Manufacturing Technology* **20**, 129-132 (May 1997).

88. Williams, D. F., Belquin, J.-M., Spisser, A., Cappy, A., and Dambrine, D., Characterisation of Coplanar Waveguide on Epitaxial Layers, *Electron. Lett.* **33** (17), 1468-1469 (August 1997).

89. Williams, D. F., Hayden, L. A., and Marks, R. B., A Complete Multimode Equivalent-Circuit Theory for Electrical Design, *J. Res. Natl. Inst. Stand. Technol.* **102**, 405-424 (1997).

90. Williams, D. F., Janezic, M. D., Ralston, A., and List, S., Quasi-TEM Model for Coplanar Waveguide on Silicon, 1997 EPEP Conference Digest, San Jose, California, October 27-29, 1997, pp. 225-228.

91. Zachariah, M. R., and Melius, C. F., Theoretical Calculation of Thermochemistry for Molecules in the Si-P-H System, *J. Phys. Chem. A* **101**, 913-918 (1997).

92. Zhang, N.-F., Postek, M. T., and R. D. Larrabee, Statistical Measure for the Sharpness of the SEM Image, Proceedings of the SPIE, The International Society for Optical Engineering, *Metrology, Inspection, and Process Control for Microlithography XI* **3050**, 375-387 (1997).